USE OF SWITCHED FABRICS IN IMPLEMENTATION OF SOFTWARE DEFINED RADIO SMART ANTENNA AND INTERFERENCE CANCELLATION SIGNAL PROCESSING

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ABSTRACT

Data flow and functional processing for smart antenna systems used with different waveforms, such as Frequency Division Multiple Access (FDMA), Time Division Multiple Access (TDMA), and Code Division Multiple Access (CDMA), differ from one waveform type to another. Adaptive antenna systems used with software-defined radio (SDR) mobile terminals and base stations must be able to reconfigure not only their waveform processing, but also their functional processing data flow. Switched fabrics using crossbar switches are ideal for real-time hardware implementation of such systems.

In like fashion, co-site interference cancellation systems used by software defined radios also demand the use of switched fabrics for implementation, providing the needed software-reconfigurable data flow for adaptive processing.

This paper examines implementation requirements of representative software defined space-time systems such as smart antennas and interference cancellation. For smart antennas and interference cancellers, low-latency and low-jitter fabrics with low wire-counts are a must. A modular, scalable implementation architecture which complies with the Joint Tactical Radio System (JTRS) Software Communications Architecture (SCA) is proposed.

1. INTRODUCTION

Software-defined radios are beginning to enter service with various defense forces around the world. For instance, the United States has procured a SDR system for its Navy called Digital Modular Radio (DMR), and recently awarded a procurement contract for a "Cluster One" tactical SDR to a Boeing-led Consortium for the Army's next-generation vehicular and helicopter radio. Both radios will comply with a US procurement specification issued by the Joint Tactical Radio System (JTRS) Joint Program Office (JPO) called the Software Communications Architecture (SCA) [1] (Figure 1).

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Some special-mission aircraft require adaptive antenna arrays and co-site interference cancellation systems to perform their missions, such as the E-2C Hawkeye (Figure 2) and AWACS.

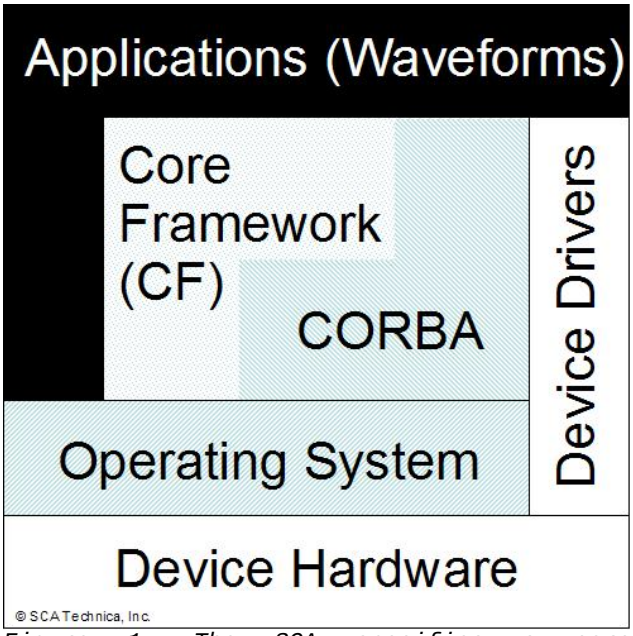


Figure 1. The SCA specifies a core framework (CF), a POSIX OS profile, and a middleware layer employing a CORBA object request broker (ORB). Interface specifications are provided for services and devices.

Figure 2. For effective communications, some aircraft such as the E-2C Hawkeye may require sophisticated adaptive processing systems such as co-site interference management systems. Use of software-defined radio communication systems in such aircraft requires use of software-defined antenna and interference management systems. (Figure: Northrop Grumman)

In these aircraft, the antenna system must be able to "null" hostile electronic countermeasure systems (ECM) as well as cancel the effects of on-board, co-site electromagnetic interference (EMI) which may impair the effectiveness of

sensitive radio receivers. Especially in the case of propeller driven aircraft, such as the E-2C, or helicopters such as the Army Airborne Command and Control System (A2C2S), sophisticated co-site interference cancellation systems are needed to mitigate the time-varying EMI effects resulting from movement of propellers and rotors. In some instances such as A2C2S, these effects can cause as much as a 30 dB amplitude modulation of the received signal at 2x or 4x the rotor frequency, resulting in severe quality of service (QoS) degradation of voice and data.

As part of the US Core Avionics Master Plan (CAMP), the radios in these aircraft are being upgraded to JTRS SCA compliant SDR. However, the use of SDR presents an additional complication in the implementation of antenna beam forming systems and co-site interference cancellation systems, requiring the use of software defined adaptive processing methods. These issues are addressed in the remainder of this paper.

2. ADAPTIVE ANTENNAS

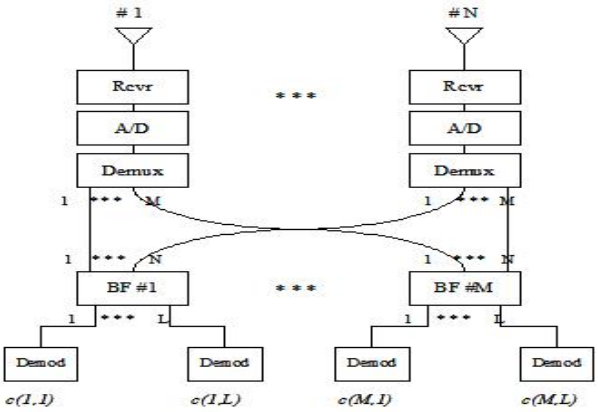


Figure 3. FDMA adaptive beam forming receive data flow.

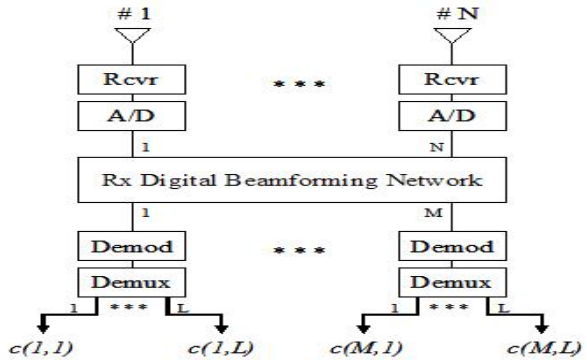


Figure 4. TDMA adaptive beam forming receive data flow.

Data flow and functional processing for digital beam forming (DBF) used with different waveforms, such as Frequency Division Multiple Access (FDMA) (Figure 3), Time Division Multiple Access (TDMA) (Figure 4), and Code Division Multiple Access (CDMA) (Figure 5), differ from one waveform type to another [2]. Note, for instance, the relative locations of the de-modulation and de-multiplexing processing between FDMA, TDMA and CDMA relative to the data flow "fan-outs". Adaptive antenna systems used with software-defined radio systems must reconfigure *both* their waveform processing *and* functional processing data flow, to accommodate different beam forming designs for multiple waveform types.

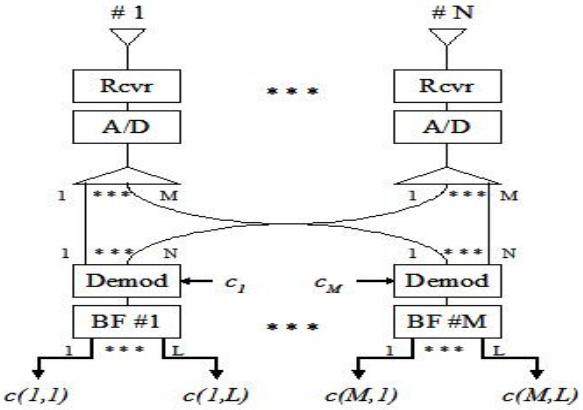


Figure 5. CDMA adaptive beam forming receive data flow.

3. CO-SITE INTERFERENCE MANAGEMENT

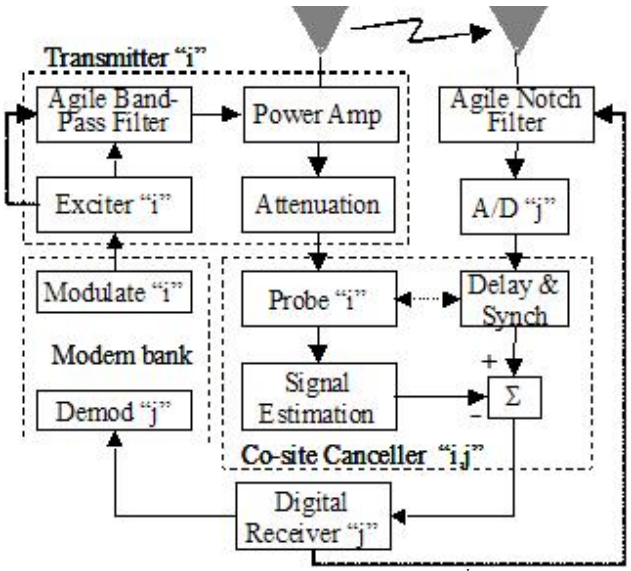


Figure 6. Functional processing diagram for i^{th} transmitter and j^{th} receiver of subtractive co-site interference canceller.

In like fashion, co-site interference cancellation systems used by software defined radios also demand the use of software-reconfigurable adaptive processing. In today's co-site interference cancellation systems, a method called "subtractive interference cancellation" is often used (Figure 6). In this method, a signal transmitted on the

platform (e.g. the aircraft) is attenuated and sampled at the i^{th} transmitter; sent through a channel estimator (which models the frequency- and time-dependent effects on the signal on the channel between the co-site transmitter and receiver); then subtracted from a time-delayed version of the j^{th} received signal (where the delay may be a function of frequency) in real time. These cancellation algorithms vary on a waveform-by-waveform and platform-by-platform basis, and are typically frequency-dependent. Thus, in a SDR system, signal estimation components of the subtractive co-site interference cancellation system must also be software defined.

On certain platforms, such as aircraft, the time-varying ground plane and multi-path effects of moving surfaces such as rotor blades, propeller blades, control surfaces, gun barrels etc. may cause additional (and significant) interference effects which must also be managed. For instance, 30 dB modulation of transmitted or received signal envelopes have been recorded on certain antennas on the UH-60 helicopter (Figure 7), causing significant loss of QoS particularly on data signals, reducing both data rate and effective communication range.

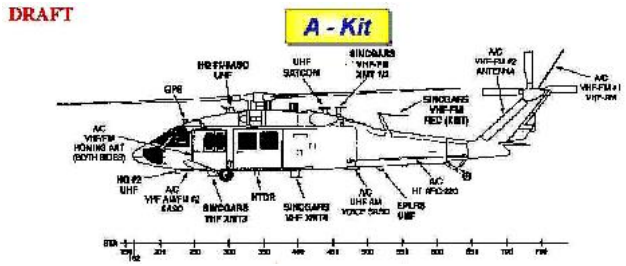


Figure 7. The Army Airborne Command and Control System (A2C2S) variant of the UH-60C Blackhawk. (Figure: US Army)

4. SWITCHED FABRICS

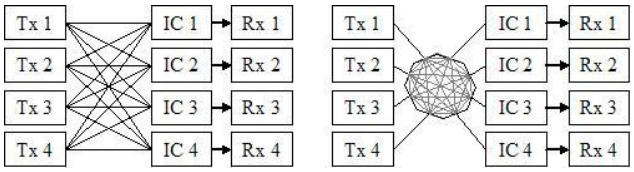


Figure 8. Data flow implementation of a subtractive co-site interference management systems is typically of complexity [i x j] for a system with i transmitters and j receivers. Use of a single 8-port crossbar switch (right) can reduce the "fan-out" to complexity [i + j], reducing both pin and wire counts.

A switched fabric is a multi-branch I/O bus employing one or more cross-bar switch, a device which provides several non-blocking logical paths between ports. Unlike traditional computer busses such as PCI, which only allows one-at-a-time communication between pairs of components, a switched fabric allows multiple simultaneous (non-blocking) communication paths. For instance, a well-designed 8-port crossbar switch allows non-blocking communications for up to 4 pairs of devices. The use of a switched fabric can significantly reduce the complexity of implementing reconfigurable co-site interference cancellation systems (Figure 8) and adaptive antenna systems.

Early crossbar fabrics were based on "parallel" I/O fabrics. For example, a 32-bit, 40 MHz, 6-port crossbar switch architecture (RACEway Interlink) was introduced by Mercury Computer Systems, Inc. and standardized as ANSI/VITA 5-1994. RACEway is a circuit-switched architecture for embedded multi-processor systems employing a Globally Shared Memory (GSM). The upgraded Race++™ architecture introduced an 8-port crossbar at optional 40 MHz or 66 MHz fabric speeds [3]. A competing 64-bit packet-switched architecture (SKYchannel) was introduced by rival Sky Computers Inc. and standardized as ANSI/VITA 10-1995 [4].

Recently introduced serial switched fabrics are better suited than parallel fabrics in wireless implementations. For example, the "common" physical layer shared by Serial RapidIO [5], Infiniband [6] and Gigabit Ethernet [7] employs low voltage differential signaling (LVDS) and requires only 4 wires to implement a fully bidirectional serial I/O port, and significantly reduce the pin and wire counts needed to implement richly connected switched fabrics. From the hardware designer's point of view, the use of a common physical layer allows the use of intellectual property (IP) cores (e.g. buffer amplifiers, etc.) for the common physical layer to be used in designs for multiple serial switched fabrics, affording excellent flexibility for designers of Serial RapidIO, Infiniband, and Gigabit Ethernet devices.

To implement front-end processing for SDR modems and adaptive processing, a technology offering compact (lowest gate-count) implementations for switched fabric endpoints and crossbars should be selected to simplify implementation in FPGA and ASIC devices. Further, a switched fabric complying with one of the open standards should be selected to satisfy the SCA requirement. Serial RapidIO, designed for compact embedded multi-processor applications (including wireless front ends) is a good choice given these constraints. The RapidIO 1x/4x LP-Serial physical layer specification has the following properties [5]: Embeds the transmission clock with data using an 8B/10B-encoding scheme; Supports one serial differential pair, referred to as one lane, or four ganged serial differential pairs, referred to as four lanes, in each direction; Allows switching packets

between RapidIO 1x/4x LP-Serial Ports and RapidIO Physical Layer 8/16 LP-LVDS ports without requiring packet manipulation; Employs similar retry and error recovery

Device	Rocket I/O Transceiver Blocks	PowerPC Processor Blocks	Logic Cells(1)	CLB (1 = 4 slices = max 128 bits)	
				Slices	Max Distr RAM (Kb)
XC2VP2	4	0	3,168	1,408	44
XC2VP4	4	1	6,768	3,008	94
XC2VP7	8	1	11,088	4,928	154

protocols as the RapidIO Physical Layer 8/16 LP-LVDS specification; and Supports transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane.

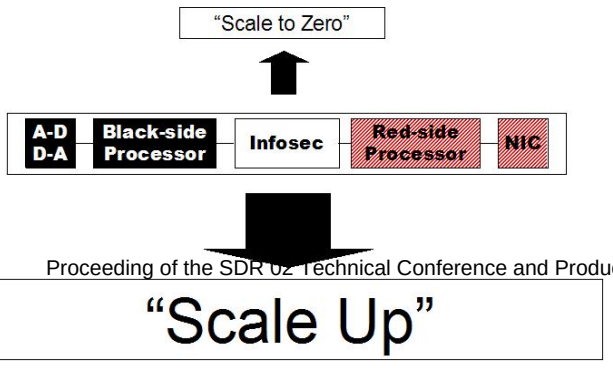
Figure 9. The XC2VP7 FPGA contains eight transceivers, used to provide gigabit I/O between the digital transceivers, modems, and adaptive processing and its host device. It also contains a PowerPC 405 32-bit RISC CPU. (Figure: Xilinx)

Figure 10. (below) The XC2VP7 FPGA comes in a package as small as 23x23 mm when packaged in FG456. This small package fits well in small wireless packages, and contains 248 user available I/O pins.

Pkg	Pitch (mm)	Size (mm)	XC2VP2	XC2VP4	XC2VP7
FG256	1.00	17 x 17	140	140	
FG456	1.00	23 x 23	156	248	248
FF672	1.00	27 x 27	204	348	396
FF896	1.00	31 x 31			396

(Figure: Xilinx)

It is worth noting that crossbar switch IP cores are available for modern ''platform FPGA'' chipsets such as the Xilinx Virtex II Pro [8]. It is also worth noting that many legacy military waveforms can be implemented using 700K gates or less. The newest generation of FPGA's can provide 700K gates, a PowerPC core, and eight LVDS transceivers in a package less than one inch square (Figures 9, 10) [9].



5. SCALABILITY

Figure 11. Early SDR models included a general purpose processor on both the "red" and "black" sides of the radio.

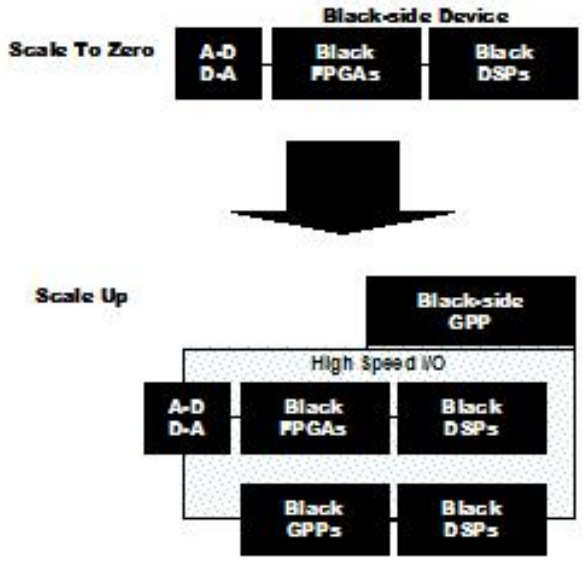


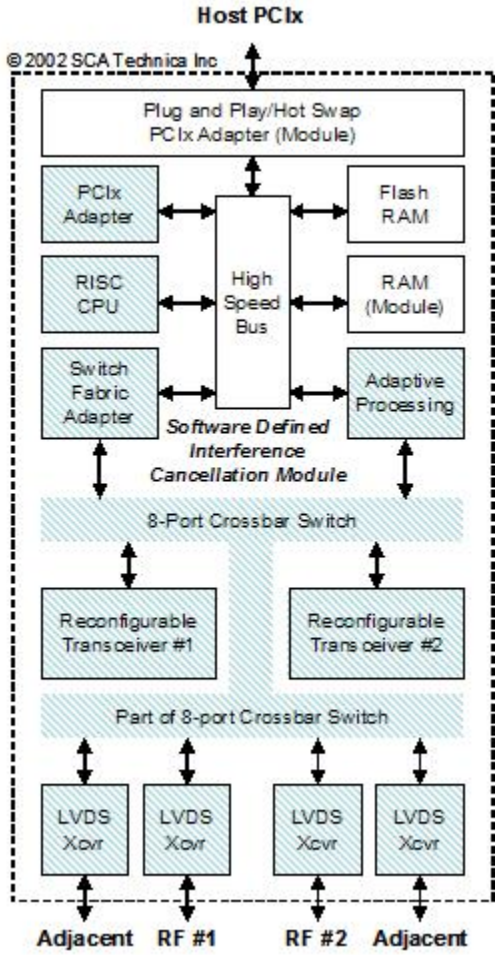
Figure 12. During the late 1990's, designers sought to reduce the cost of SDR's by employing early generation "million gate FPGA's" and eliminating the black side processor. While use of the FPGA's reduced the cost and power consumption of these radios, waveform portability.

One of the most difficult issues facing designers of SCA compliant modules is scalability. The generalized model of an SCA compliant software radio contains both "black side" and "red side" processing, separated by a security module (Figure 11). The "black" side processing treats information already protected by encryption and other security, and contains the modem signal processing and "chip" level processing including digital adaptive beam formers, Rake receivers, and interference cancellation processing.

In early SDR, both the "black" and "red" sides contained a general purpose processor (GPP), each running GPP hosting a POSIX compliant operating system (OS) kernel. By adopting a CORBA platform, the architects of these early SDR's attempted to achieve platform neutrality.

More recent design attempts done in the late 1990's sought to eliminate the GPP from the "black" side to save cost, using instead FPGA and/or digital signal processor (DSP) devices without the GPP (Figure 12). This was to save weight, cost and power by employing the early-generation "million gate FPGA's" such as the Xilinx Virtex II. However, this had some dramatic (and negative) effects on application portability on the SCA platform. Lack of a GPP meant lack of a POSIX compliant OS (as

defined by SCA Appendix B, Application Environment Profile (AEP)). This in turn meant lack of a "black" side object request broker (ORB). As a compromise, SCA designers resorted to treatment of the entire black-side signal processing as an "SCA device", essentially treating



the reconfigurable "black" side components as hardware. The dream of platform-neutral waveforms was lost – at least temporarily.

Figure 13. Possible implementation of a scalable "core module for SCA compliant SDR with built-in adaptive processing module, usable for co-site interference cancellation, beam forming, adaptive equalizers, etc.

Such compromise may no longer be necessary. As noted previously (in Section 4; Figures 9-10) the new "platform" FPGA's offer the necessary number of gates, up to eight high performance serial transceivers, a 32-bit RISC core and more in a compact package of than 23mm x 23mm. Also, devices with up to 10 million gates are available in larger package sizes. Industry estimates for implementation of a SDR modem for "legacy" military waveforms range from 700K to one million gates. Thus the implementation of two SDR modems, adaptive processing, switched fabrics, LVDS transceivers, crossbar switch, 32-bit RISC GPP and other components may be accomplished using a *single FPGA device*.

6. IMPLEMENTATION ARCHITECTURE

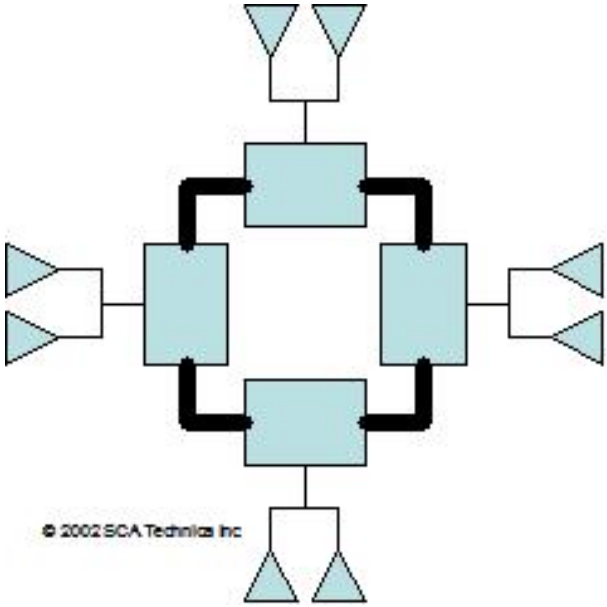


Figure 14. The "core module" with dual channel SDR modems, adaptive processing and switched fabric can be combined with other core modules to form arrays. An 8-element SDR array using four core modules is shown. If richer networking is needed, a single 8-port external Serial RapidIO (or other standard) crossbar switch may be employed. Additional units for adaptive processing may also be added to this configuration.

Given the availability of "platform" FPGA's with up to 10 million gates per device, as well as available cores for RISC processors, DSP cores, crossbar switches, clock locked transceivers, Viterbi decoders and other codecs, and other components, it is feasible today to design a scalable core module (Figure 13) for a two-channel SDR modem with built-in adaptive processing and GPP. The core module implements two LVDS ports, one PCIx port, and other external interfaces conforming to open standards such as Serial RapidIO or Gigabit Ethernet. Such a core module, with its GPP, can be designed to be a *self-booting* SCA component, and can be used in combination with other core modules, crossbars, and processors to form software defined smart antennas, co-site interference management systems, and other complex SDR systems-of-systems. Compact versions of the core module may be implemented in form factors as small as PCMCIA (*110x54x7 mm)* provided the implementation requirements of the modem and adaptive processing are kept modest (say, to one million gates per modem or less). One important implementation consideration is low jitter and clock-locked performance. For adaptive beam

forming and interference cancellation, timing precision is directly related to the effectiveness of the algorithm. Timing accuracy to nano-second accuracy is required.

7. FOR FUTURE RESEARCH

Hardware and software prototypes of a simple two-channel SDR with built-in adaptive interference management should be prototyped, using the architecture of the proposed "core module". Developed versions of the prototype "core module" might be usable as a component for a hand-held military or commercial mobile terminal. Following demonstration of a successful prototype, scalability of the core module should be demonstrated by experimentally implementing a system-of-systems such as a base station smart antenna, or a co-site interference management system for a mobile platform such as the E-2C Hawkeye or UH-60C A2C2S. Research and development of advanced concepts, such as use of observer-based compensators (Kahlman filters) for signal estimation (Figure 15) should also be investigated.

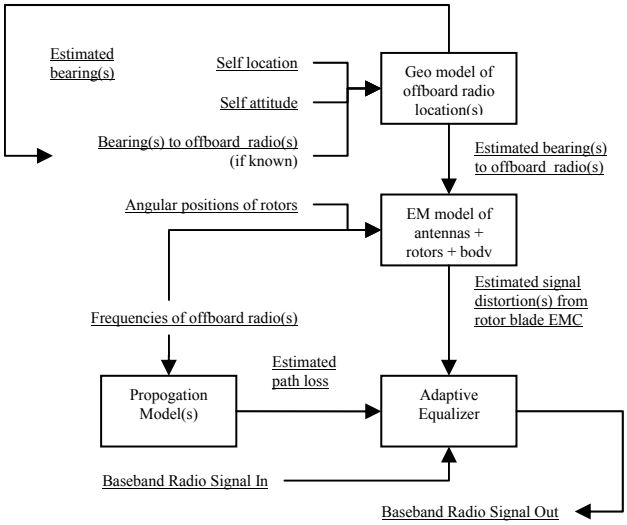


Figure 15. Possible use of observer based compensators in the airborne signal estimation function should be investigated.

8. SUMMARY

SDR has begun to enter service with the US Military and other defense units world-wide, and have also begun entering the commercial service. Some military and commercial platforms, such as special mission aircraft and wireless base stations, have requirements for advanced antenna and interference management signal processing.

In this paper we examined examples of digital adaptive beam forming and co-site interference cancellation functional data flow. In the case of adaptive beam forming, we observed that transition of the waveform from FDMA to TDMA to CDMA resulted in significant dataflow changes. In the case of co-site interference cancellation, we also determined that signal estimation of the subtractive cancellation estimate was based in part on the characteristics of the waveform being sampled (and cancelled). Thus, digital adaptive beam formers and interference management systems used with SDR systems must themselves be software-defined.

By analysis, we investigated the implementation of scalable, software defined adaptive beam forming and interference cancellation systems. We showed how use of switched fabrics can simplify implementation of software defined adaptive processing, reducing pin and wire counts from {O: i x j} to {O: i + j}. We further suggested an implementation of the switched fabric jointly with the SDR modem and adaptive processing directly on modern "platform" FPGA's without the use of external crossbars. Finally, we showed by analysis how modern "platform" FPGA's with embedded RISC processors and serial clock-locked transceivers may be used to instantiate a scalable "core" module jointly implementing SDR modems, adaptive processing and switched fabrics.

8. REFERENCES

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