GENERAL DYNAMICS
Decision Systems

20 YEARS of ALTERA® INNOVATION

Synthesizing FPGA Cores for Software-Defined Radio

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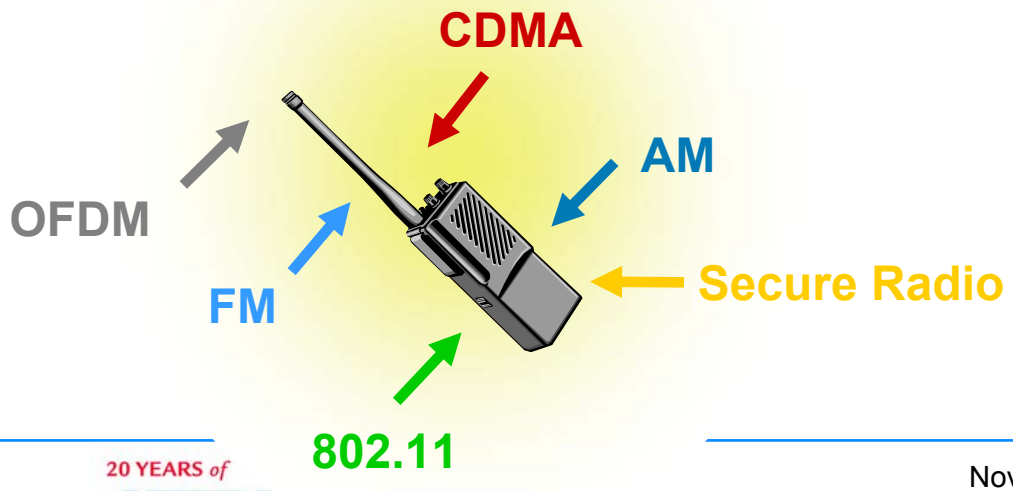
Agenda

- Background of Software-Defined Radio (SDR)
- Move to Digital Radio Architectures
- Digital Intermediate Frequency (IF) Processing
- Implementing Spread Spectrum Waveform (SSW) on FPGA
- Example of System Implementation
- Conclusions

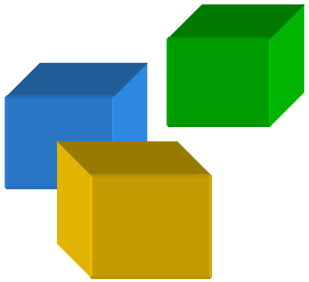
Background of SDR

- Why SDR?
  - Any Waveform, Any Time
  - Many Waveforms
  - Small Form Factors (Size, Weight, Power)
  - Unified Architecture



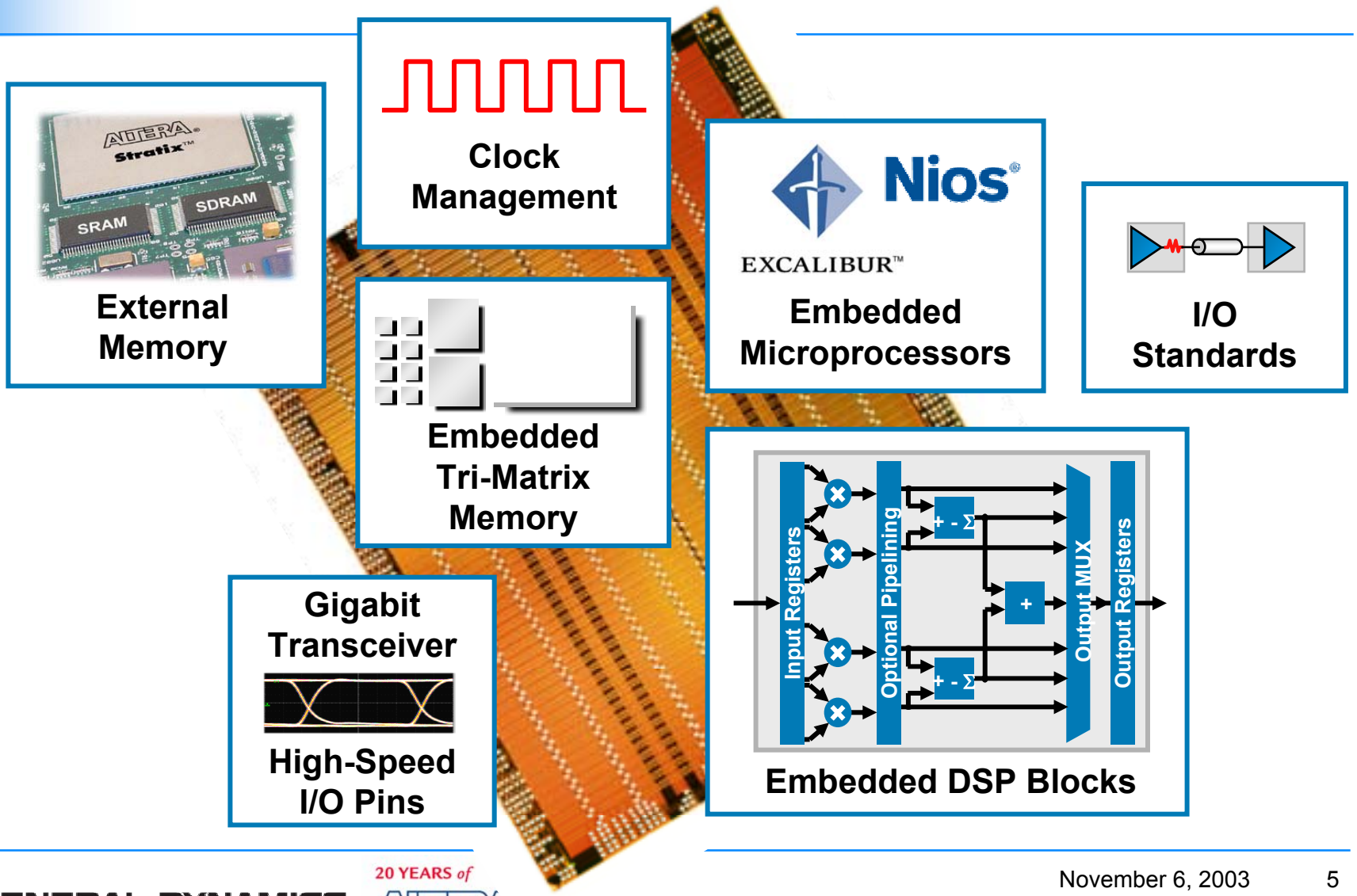
Why FPGAs for SDR?

- Building Blocks for SDR
  - Microprocessors
  - DSP Capability
  - Multiple Clock Domains
  - Multiple (& Configurable) External Interfaces



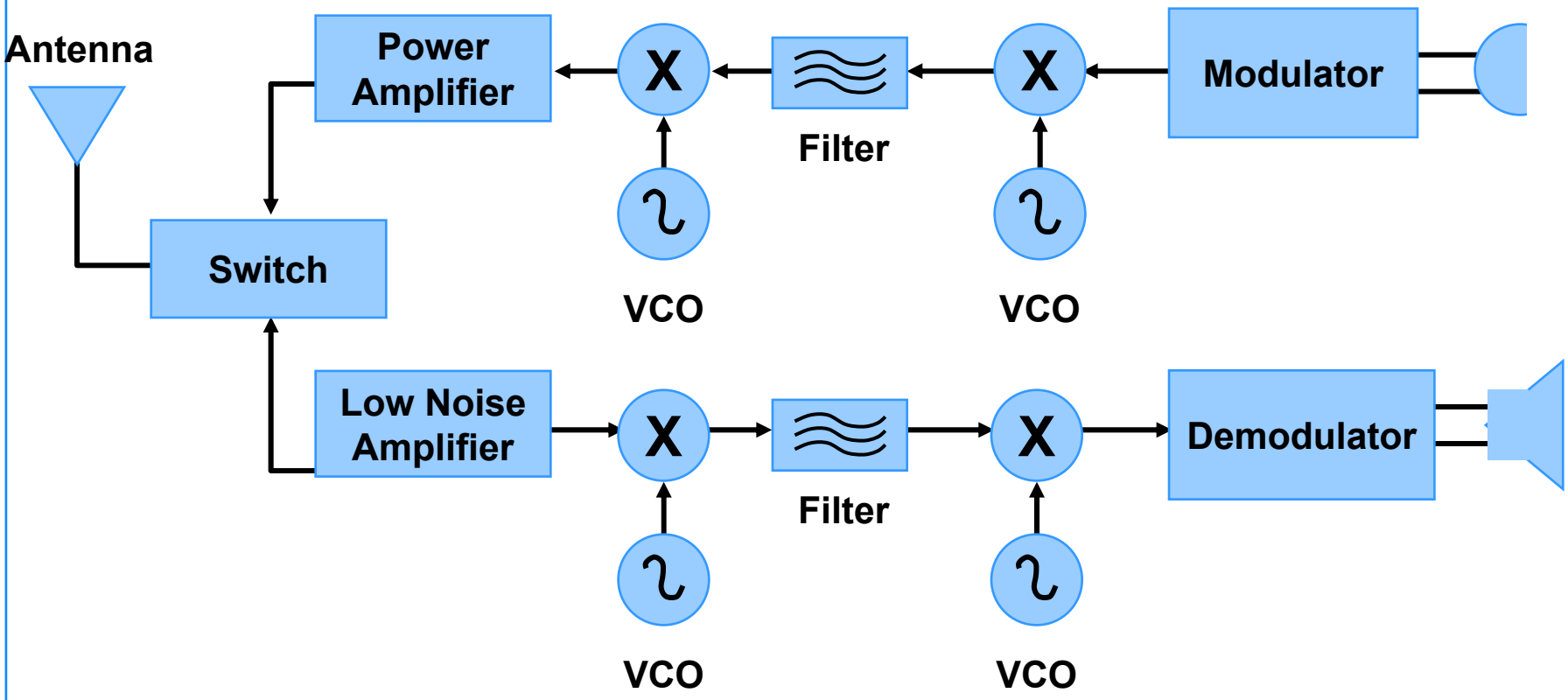
- FPGAs Have All of These
  - Soft Microprocessor Cores
  - DSP Functionality (Multipliers, Etc.)
  - Phase-Locked Loops (PLLs)
  - Configurable I/O Pins

Altera Hardware-Features for SDR



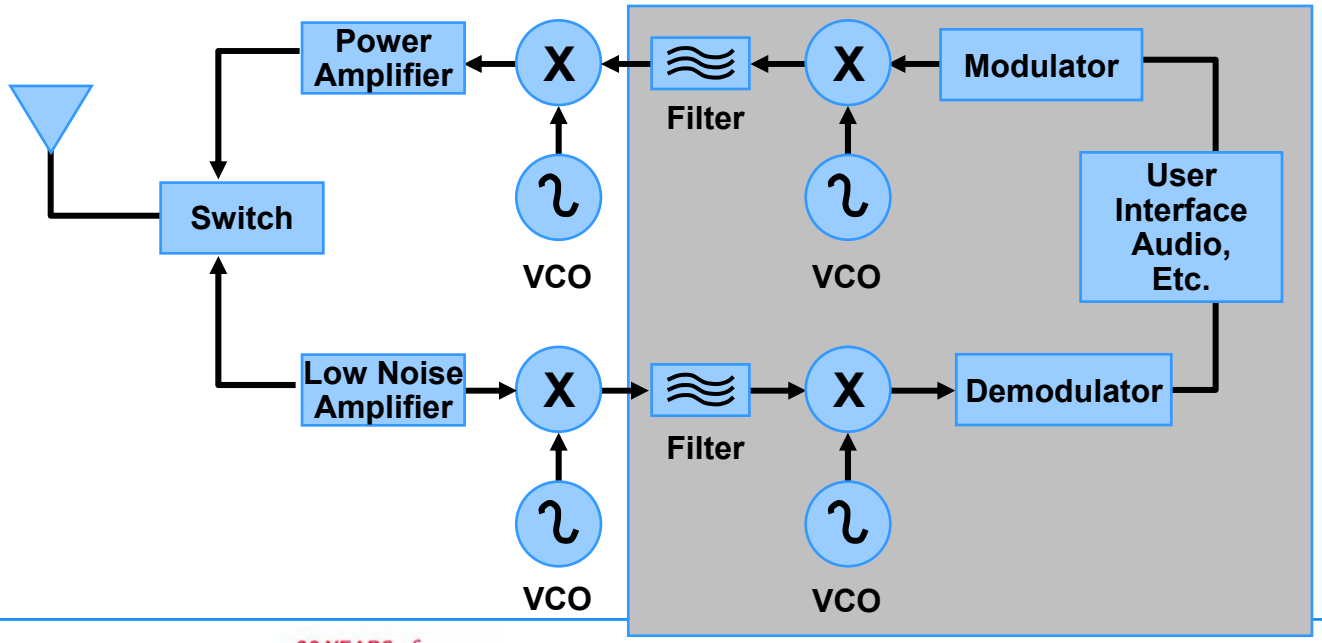
FM Radio Example

- First FM Radio
  - All Analog Implementation



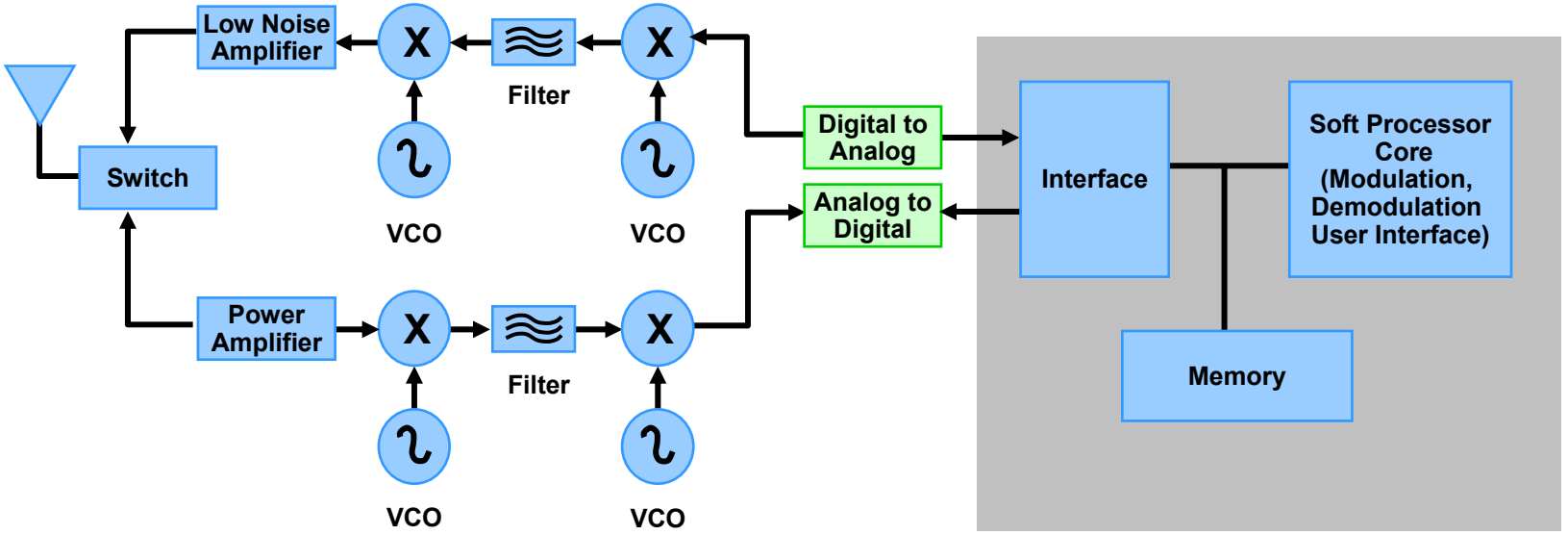
Moving to Digital Radio Architectures

- Digital Radio Has Benefits over Analog
  - Better Manufacturability
  - Lower Cost
  - No Need to Tune
  - Consistent Behavior over Power/Voltage/Temperature



Processor-Based Demodulation

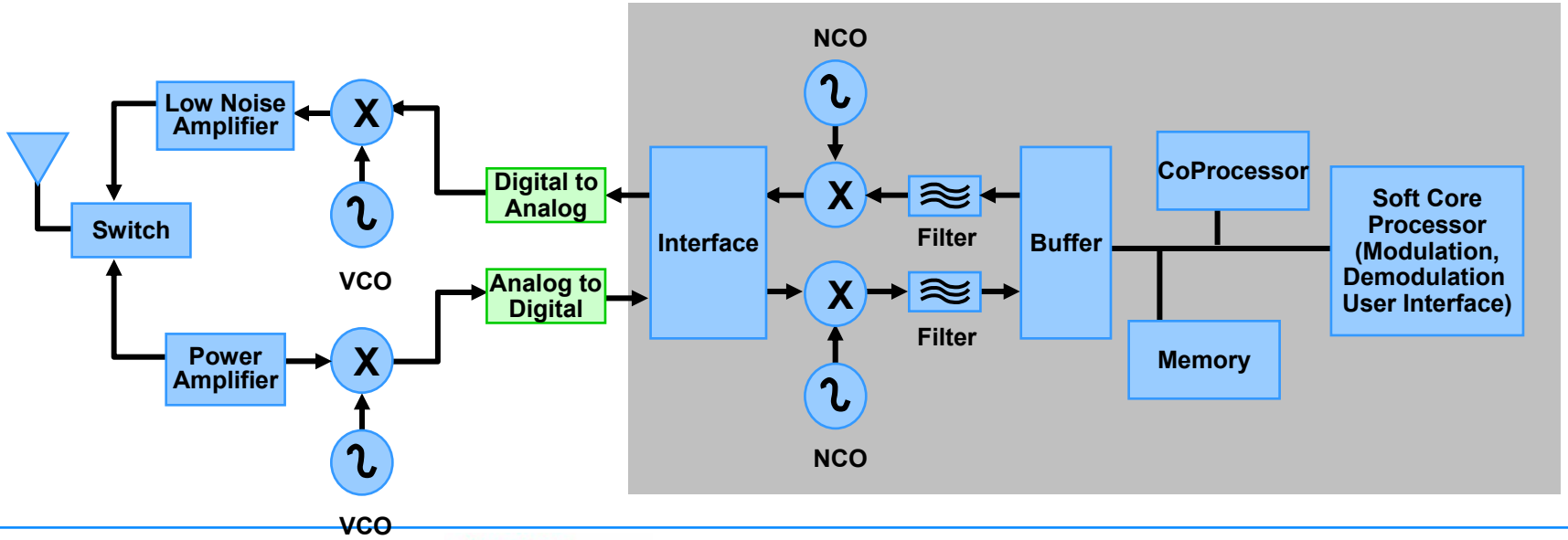
- Analog Functions Are Simply Mathematical Equations
  - Θ = arc tan(Q/I)
- These Functions Can Be Performed by Microprocessors
  - For Low Bit-Rate Signals



Improving Demodulation Speed

- Soft Core Processors
  - 100 – 200 MIPS Performance
  - Custom Instructions
- Offloading the Processor
  - Co-Processors for Specific Functions
  - CORDIC, FFT, Encryption, etc.

Function	Speed
Soft Core (Altera NIOS)	100 MHz
CORDIC	219 MHz



Digital IF Processing

- Current Generation FPGA Can Perform Digital IF Processing
  - Data Rates up to 300 MHz
  - Bandwidths up to 150 MHz
- Digital Implementations of Standard Analog Functions
  - Numerically Controlled Oscillator (NCO)
  - FIR Filters
  - CIC Filters

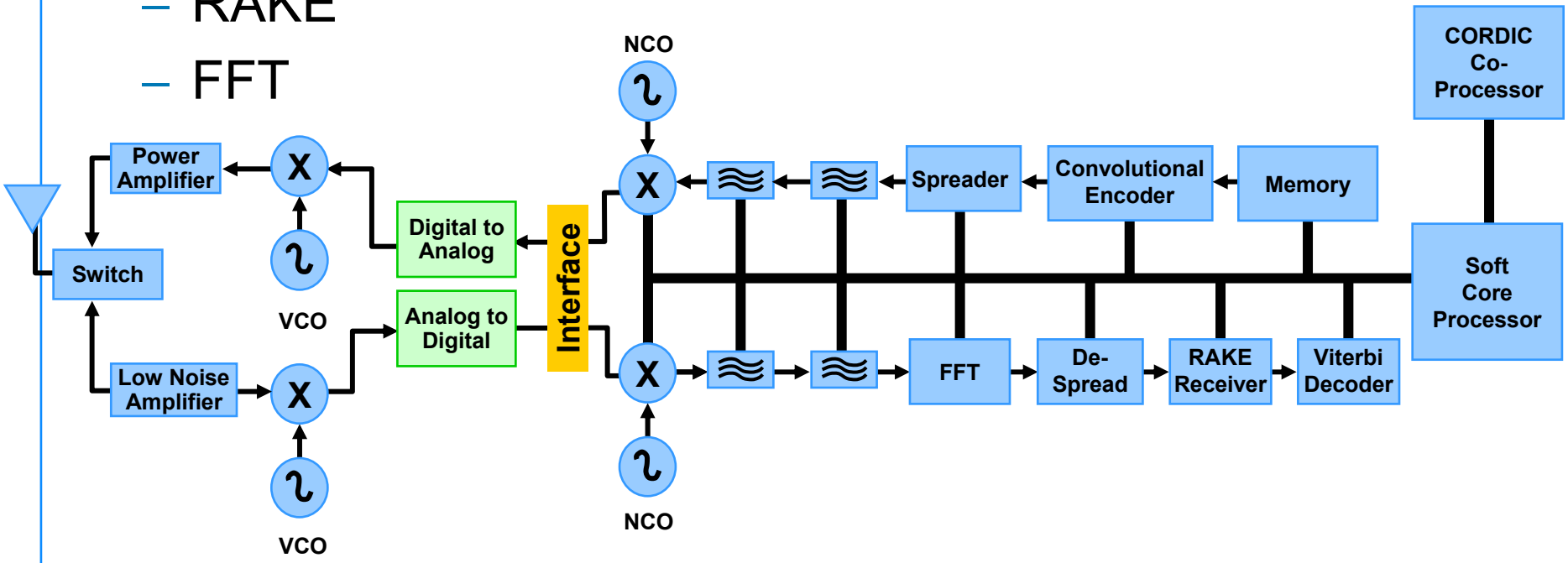
Cores for Digital IF Processing

Function	Speed	Logic Elements	Multipliers	Memory (M4K)
Parallel FIR (48 Taps, 14-Bit)	244.26 MSPS*	1,375	0	30
Serial FIR (48 Taps, 14-Bit)	19.33 MSPS*	360	0	6
NCO (24-Bit)	278.78 MHz	67	8	12
CIC (6th Order, 14-Bit)	200 MHz	1,138	0	0

* Million Samples per Second

Implementing SRW on FPGA

- Soft Processor Core for Control
- Co-Processing Engines
  - FEC
  - RAKE
  - FFT



Cores for SRW Implementation

Function	Speed	Logic Elements	Multipliers	Memory (M4K)
FFT* (128 Points)	1.03 µsec	4,838	9	19
FFT* (2,048 Point)	8.38 µsec	7,952	18	44
FFT* (8,192 Point)	38.73 µsec	8,388	18	176
Viterbi Decoder**	10 Mbps	2,600	0	0

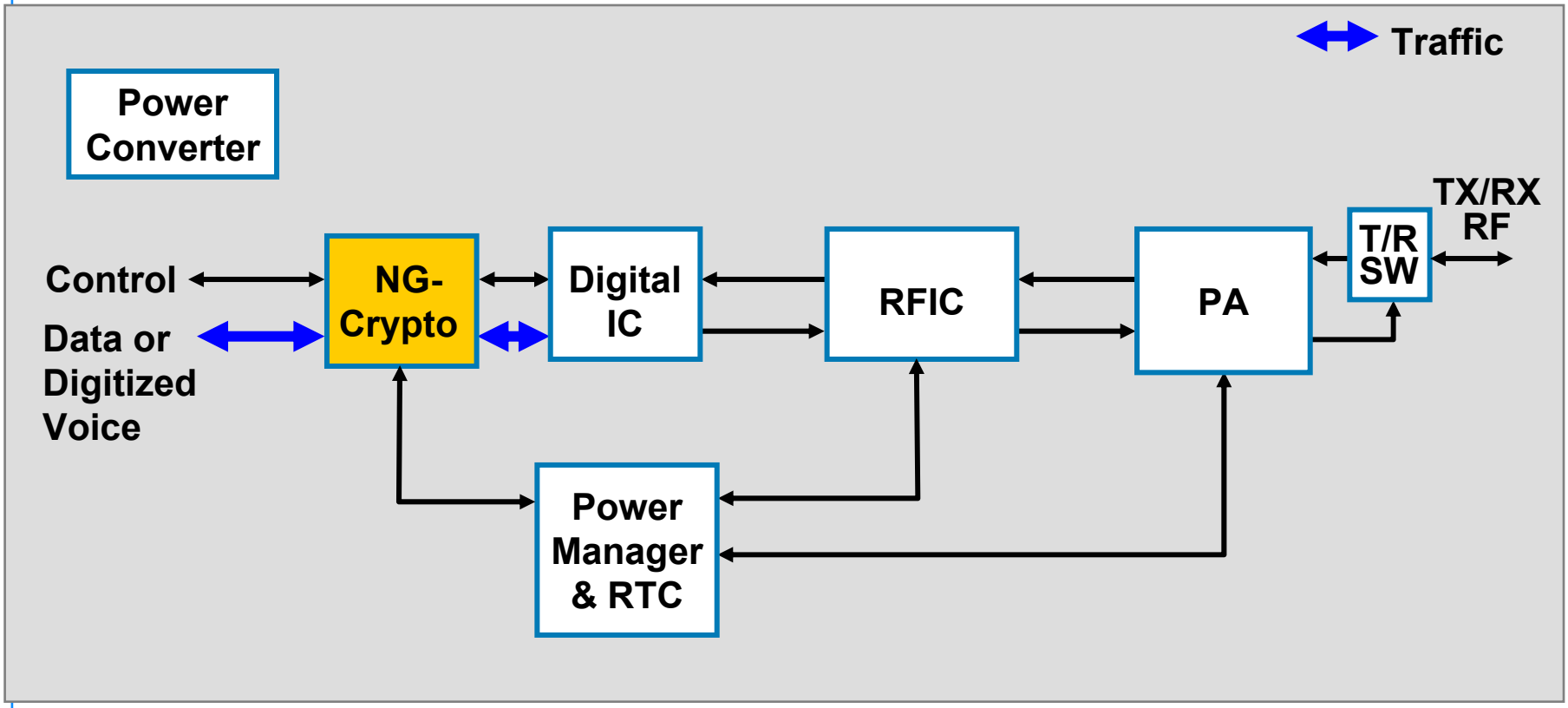
* Two Radix 4 Engines, 16-Bit Operation

** Constraint Length = 7, Number ACS = 8

Example of System Implementation

- Small Form Factor Prototype
- 5 Square Inches
- 14 Layers
- HMI Using HP IPAQ Model 5550

SDR Ideal Implementation



Conclusion

- FPGAs Are Excellent for SDR
- Combination of Resources Provide SDR Platform
  - Soft Processor Cores
  - Baseband Co-Processors
  - Digital IF Co-Processors
- Small Form Factors Can Be Achieved
  - Meeting Power/Size Requirements for Handheld Radio