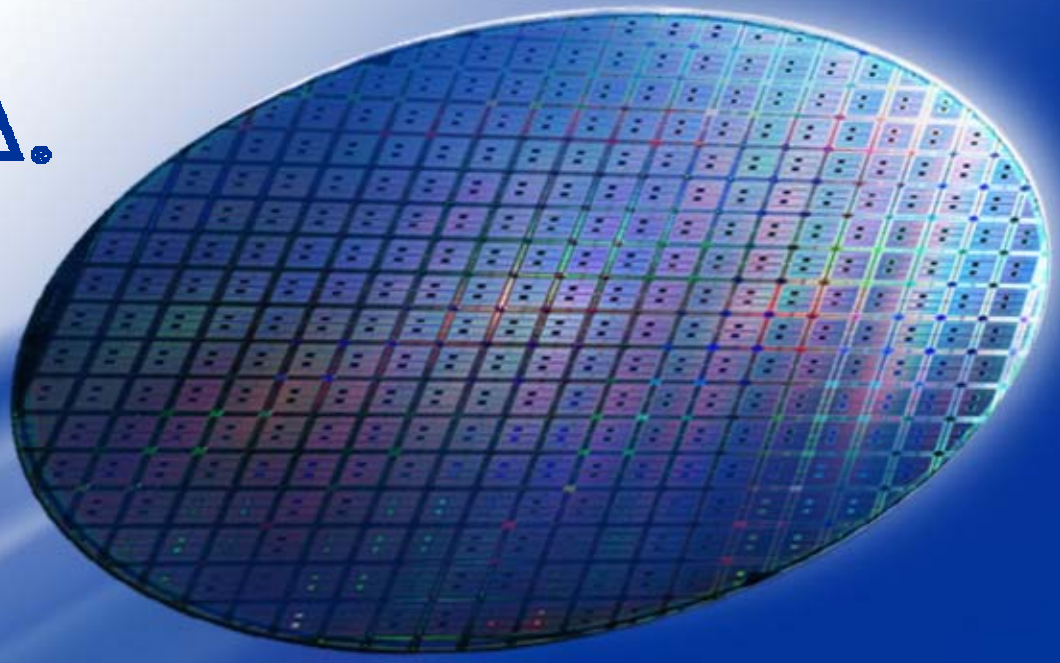

Wideband Modem Design Using FPGAs

Rob Pelt

Altera

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Outline

- Analog Up Conversion
- Digital Up Conversion (DUC)
- Polyphase Digital Up Conversion
- Conclusion
- Questions

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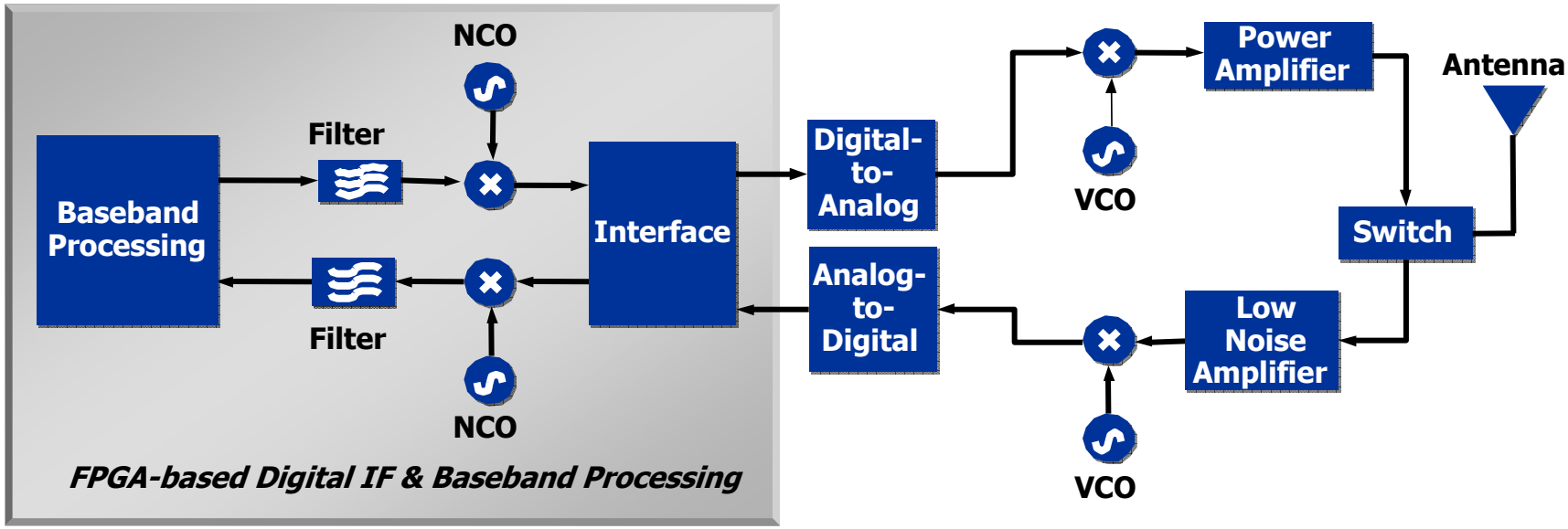
Analog Up Conversion

- Current Modems
  - Digital Baseband
  - Digital Intermediate Frequency (IF) → *Possibly*
  - Analog RF (Possible Direct Up Conversion)



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Analog Digital Up Conversion

- Impairments are Introduced
  - High Order Mixing Products
    - 3^{rd}, 5^{th}, 7^{th}, . . . Order Terms
  - Error Vector Magnitude (EVM) Impairments
    - I/Q Phase & Magnitude Imbalance
  - Carrier Feed-through
  - Harmonics
  - Sideband Noise
- Analog Filter Characteristics
  - Non-Linear Phase
  - Group Delay Variation

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Moving from Analog to Digital

- Advantages
  - Higher Performance
  - Lower Implementation Loss
  - Time to Market
  - Flexibility
- Disadvantages
  - Incremental Cost
  - Higher Power

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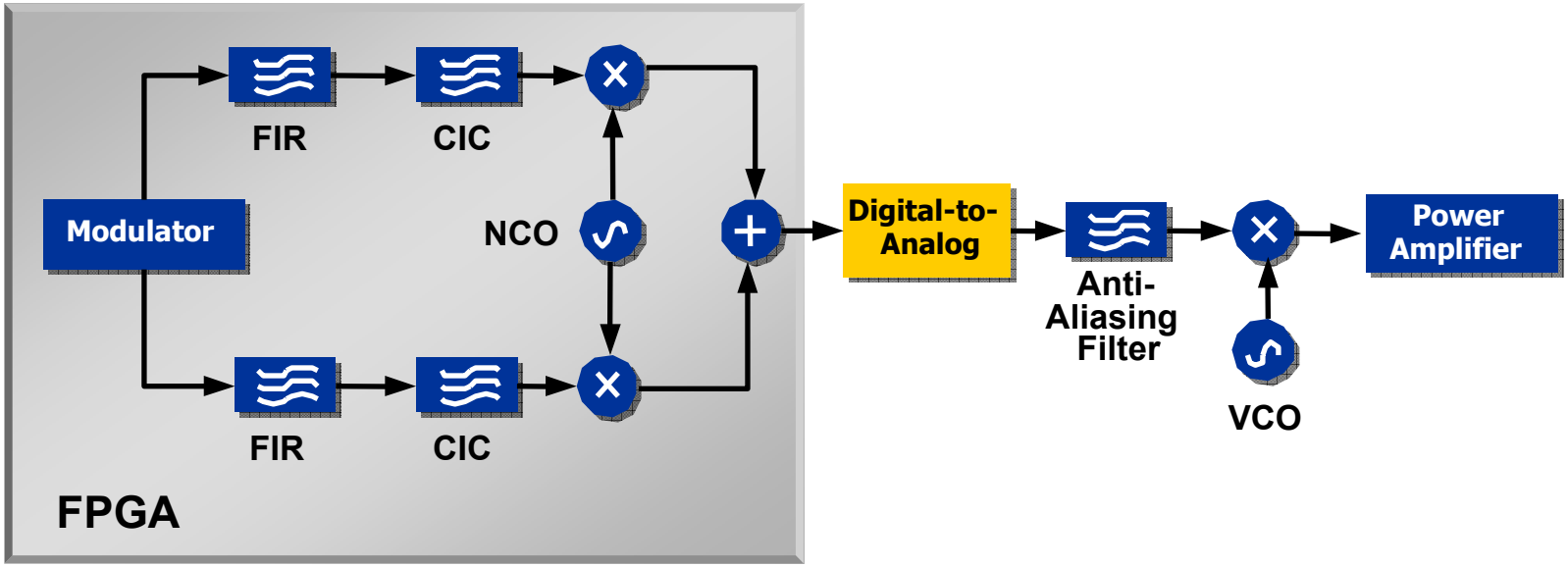
Digital Up Conversion

- Quadrature Digital IF
- Eliminates I/Q Imbalance (EVM Distortion)
- Single D/A Converter



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Digital Up Conversion in FPGA

- Current FPGAs are Feature Rich
  - Arithmetic Operators
  - Embedded Memory
  - High-Speed I/O
  - PLL
- FPGA Clock Speeds are >300 MHz
  - Bandwidths up to 150 MHz

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Altera's Stratix II FPGA Family

Device	Equivalent Logic Elements	Total Memory Bits	18x18 Multipliers	PLL
EP2S15	15,600	419,328	48	6
EP2S30	33,880	1,369,728	64	6
EP2S60	60,440	2,544,192	144	12
EP2S90	90,960	4,520,448	192	12
EP2S130	132,540	6,747,840	252	12
EP2S180	179,400	9,383,040	384	12

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Digital Up Converter

- Stratix II Common Building Blocks
- Speeds at >300 MHz
- Nyquist Bandwidth of ~150 MHz

Component	Maximum Speed
FIR Filter	339 MHz
NCO	404 MHz
FFT (256 point)	314 MHz

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Polyphase Approach

- Current D/A converters Have Sample Rates of >1 GSPS
  - Bandwidth of >500 MHz
- Standard DUC Approaches Limit Bandwidth to ~150 MHZ
- Polyphase DUC can Take Advantage of D/A Sample Rates
  - Bandwidths up to DAC Nyquist

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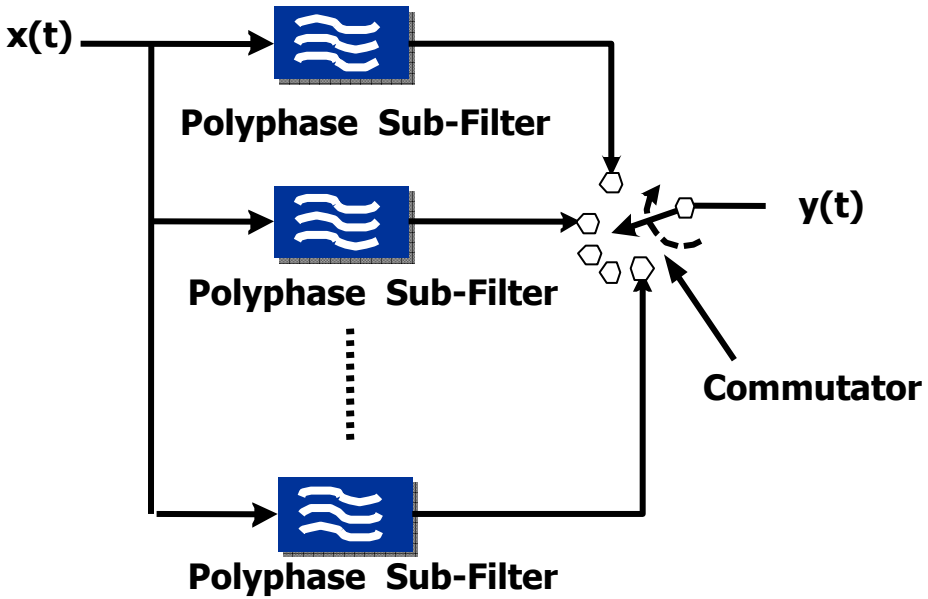
Polyphase Approach

- Familiar Polyphase Decomposition
- Each Sub-Filter Processes a Different Phase of the Input Signal
- Output Commutator Supplies Up-Sampling



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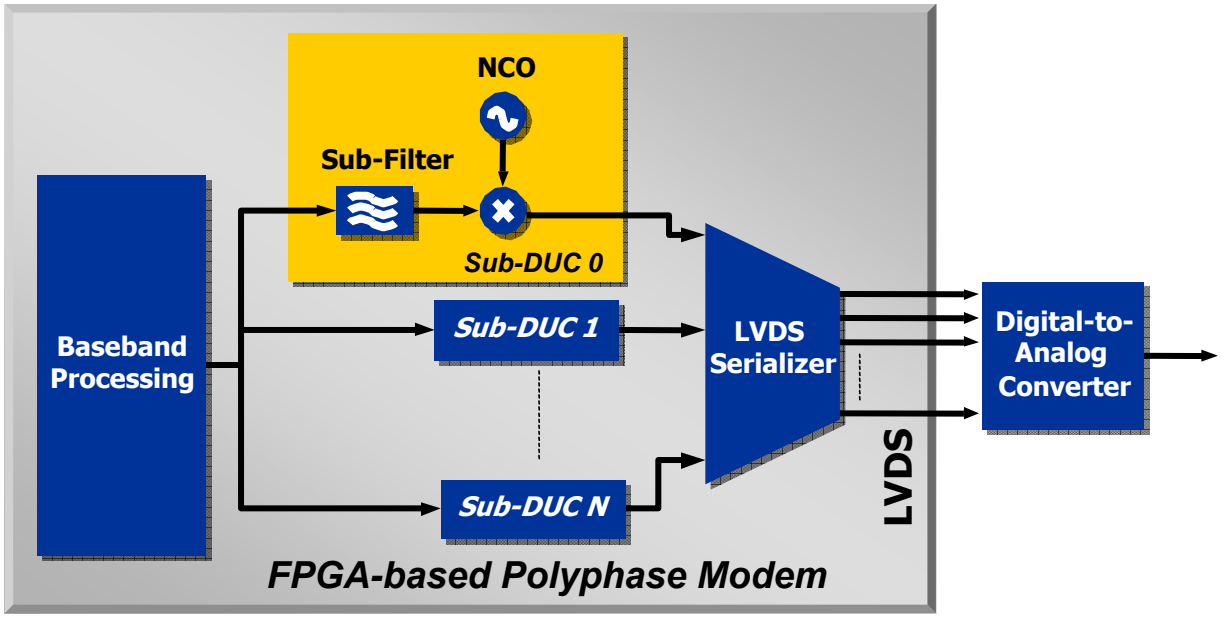
Polyphase Digital Up Conversion

- Polyphase Decomposition of Up-Conversion
- *Sub-DUC* Replaces Sub-Filters
- Low Voltage Differential Signaling (LVDS)
  - Serializer Mux
  - Replaces Commutator



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Sub-DUC Construction

- Mixer
- Filter
  - Normal Polyphase Decomposition
- NCO
  - Frequency
  - Initial Phase
  - Spectral Inversion Compensation

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NCO Frequency

- Set frequency Based on Desired Alias

$$F_{a\_gen} = \begin{cases} F_{gen} & \text{for } F_{gen} < F_{s\_nco}/2 \\ F_{gen} - (F_{s\_nco} * alias) & \text{for } F_{gen} > F_{s\_nco}/2 \end{cases}$$

Where:

Fa_gen is alias frequency setting for the NCO
Fgen is the desired output frequency
alias is the Nyquist zone number

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NCO Phase

- Phase Set for Alias Frequency

$$\phi_N = \frac{360 * F_{gen}}{F_{s\_dac} * N}$$

Where:

N is the number of sub-DUCs
Fs_dac is the clock speed of the DAC
Fgen is the desired output frequency

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Conclusion

- FPGAs are Well Equipped for Digital Up Conversion
- D/A Converters with GHz Sampling Rates are Available
- Using Polyphase Decomposition & Aliasing, FPGAs Can Be Used to Interface to the GHz D/A Converters

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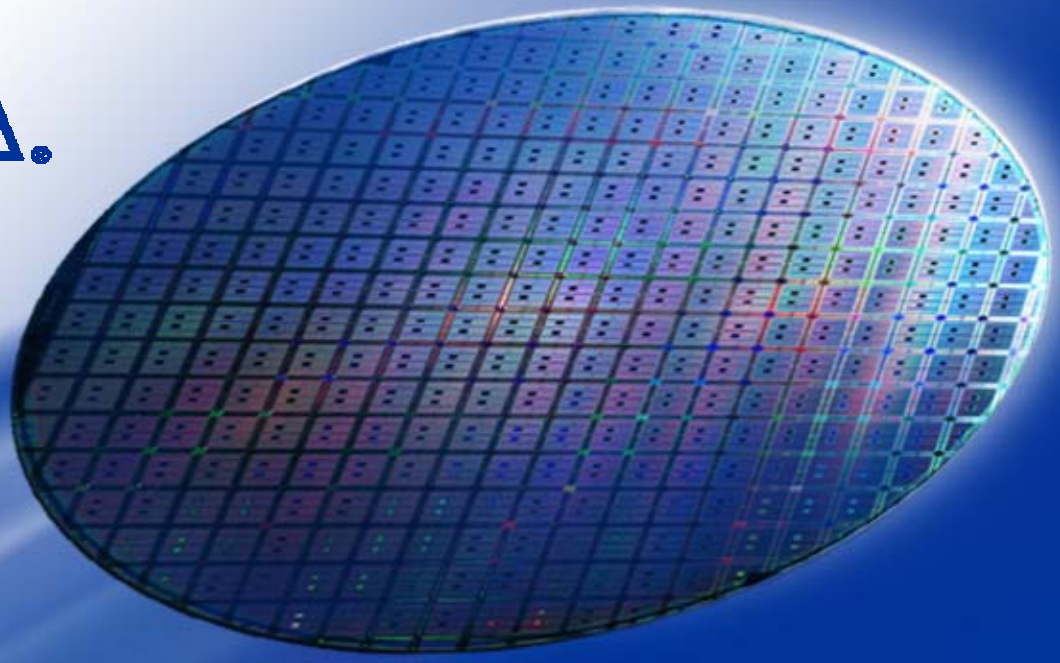

Thank You

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