RECONFIGURABLE OSCILLATOR AND FILTER

Deepak Domalapally, Jianning Wang and Yumin Zhang
School of Electrical and Computer Engineering
Oklahoma State University, Stillwater, OK 74078

ABSTRACT

Digital VCO and reconfigurable filter circuits are designed, and their functions are simulated in CMOS SOI 0.25μm process using Cadence spectre RF. A digital varactor is realized by using a parallel and series combination of capacitors. The oscillator can be tuned to different discrete frequencies depending on the digital control word. On the other hand, the filter can be reconfigured to one of the four types of basic filters by means of a digital control word.

1. INTRODUCTION

With the rapid progress of software-defined radio, digital voltage-controlled oscillator (VCO) and reconfigurable filter attracted considerable attention [1]-[3]. On the other hand, as passive elements occupy much larger area than active circuits on a semiconductor chip, it is desirable to make full use of these passive elements. Therefore, it is ideal to construct different functional circuits with the same set of passive elements.

VCO is an important device in communication systems, where the oscillation frequency can be controlled by an analog voltage signal. However, if discrete oscillation frequencies are needed, one can use digital signal to control it. A commonly adopted circuit is the parallel capacitor bank, which can generate all the parallel combinations of the binary capacitors. In this paper we adopted a switching matrix approach, where both parallel and series combinations can be implemented.

Filter is another important device in communication systems and there are four basic types of filters: low-pass (LPF), high-pass (HPF), band-pass (BPF) and band-stop (BSF). All these filters can be implemented as different combinations of capacitors and inductors. Therefore, these filters can be dynamically reconfigured with a switching network connected with a bank of inductors and capacitors.

2. Digital VCO

2.1 LC VCO Core

Fig. 1 shows an LC oscillator core, which is implemented as a cross coupled PMOS-NMOS oscillator. This circuit has the advantage of higher transconductance and output voltage amplitude compared to the oscillator circuit where only NMOS or PMOS are used.

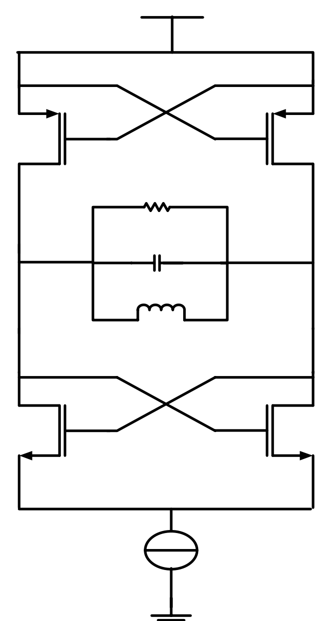

Fig. 1. Complementary cross coupled LC oscillator.

The oscillator start up condition is given by $R_o>2/g_{meff}$, where $g_{meff} = 0.5(g_{mp}+ g_{mn})$ and $g_{mp,}$

g_{mn} are the transconductances of the NMOS and PMOS transistors, respectively. The transistor widths are accordingly chosen such that $g_{meff}R_o>3$, in order to makes sure the oscillation can get started. In the above circuit Ro is explicitly shown as the equivalent parallel resistance of the series resistance of the inductor.

2.2 Switching matrix capacitor circuit

A general approach to get wide range of discrete tuning frequencies is by switching a parallel bank of capacitors [4]. The switching matrix capacitor circuit presented in this paper utilizes both the parallel and series combinations of the capacitors. The switches are controlled by digital input. Fig. 2 shows a two bit switching matrix capacitor circuit.

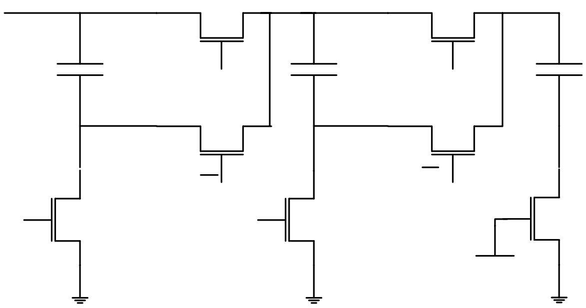

Fig. 2. Switching matrix capacitor circuit

The capacitor C is 1 pF; the gate length is 0.5 um, and the widths of the p- and n-MOSFETs are 1mm and 0.5 mm, respectively. In this circuit wide MOSFETs have to be employed in order to reduce the on-resistance. Compared with the conventional configuration with a bank of parallel capacitors, a wider tuning range can be obtained at the expense of increased power dissipation and slight degradation of phase noise.

2.2 Simulation Result

The digital VCO is simulated using Cadence spectre RF, the results are shown in Fig. 3. The simulation shows that a wide tuning range of 25% around the centre frequency can be achieved with four capacitors. When all the capacitors are connected in parallel the frequency is observed to be 1.44GHz. On the other hand, when all the capacitors are connected in series the VCO oscillates at 1.8GHz.

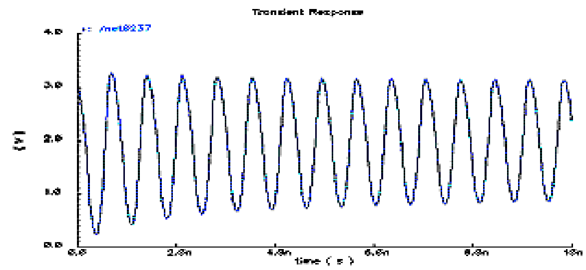

Fig. 3. Transient response of oscillator

The phase noise is also simulated, which is shown in Fig. 4. It is 106dBc/Hz at 600 kHz offset. For different combinations of capacitors, the phase noise basically remains the same.

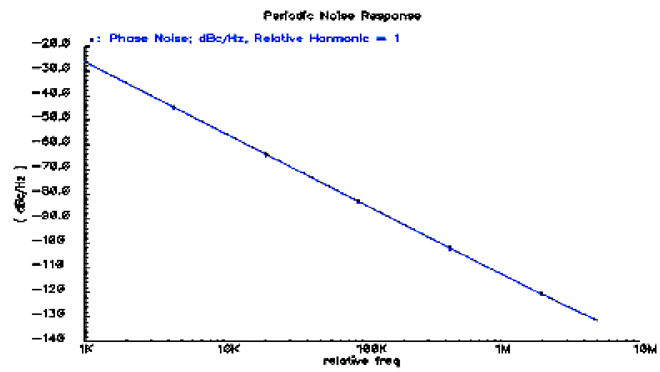

Fig. 4. Phase noise of the oscillator circuit

3. RECONFIGURABLE FILTER

3.1 Filter Circuit

The reconfigurable filter presented in this paper consists of two inductors and two capacitors, with the values of 5 nH and 3 pF, respectively. The reconfiguration here is again realized by using a switching network. Depending on the digital control inputs to the switching network, the filter can be reconfigured to one of the four types of basic filters. Fig. 5 shows the circuit diagram of filter.

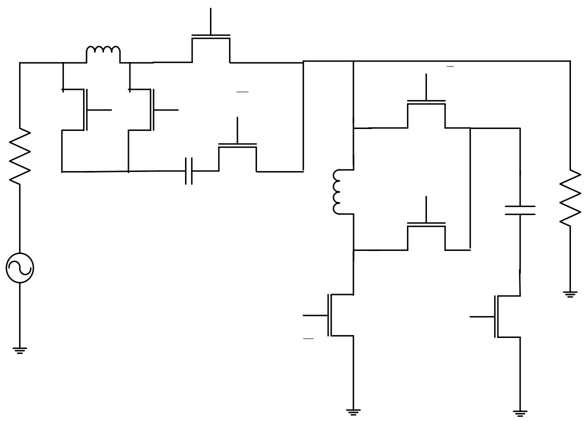

Fig. 5. Reconfigurable filter

The correspondence between the digital control word and the filter type is shown in the table below:

Table I Reconfigurable Filter

Type of filter	Digital word $b_3b_2b_1b_0$
Low Pass	0100
High Pass	0001
Band Pass	0010
Band Stop	1011

Because each MOS switch contributes to the attenuation of the input signal with its finite on resistance, the width of the switching MOSFET must be chosen accordingly to reduce this penalty. On the other hand, the transistors cannot be made arbitrarily wide either, because the parasitic capacitances can change the operation of the circuit. In this circuit the width of the MOSFETs is 50 um, and gate length is 0.5 um.

3.2 Simulation Result

Fig. 6-9 are simulation results of these four kinds of filters, respectively. For the LPF and HPF the corner frequency is in the GHz region, as well as the center frequency of the BPF and BSF filters.

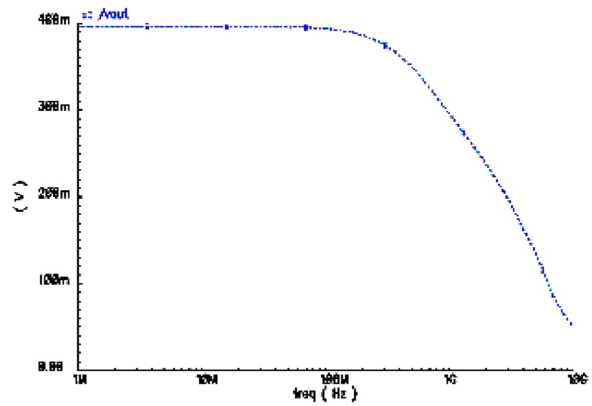

Fig. 6. Frequency response of low pass filter

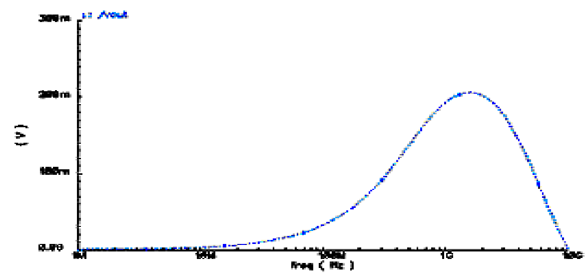

Fig. 7. Frequency response of band pass filter

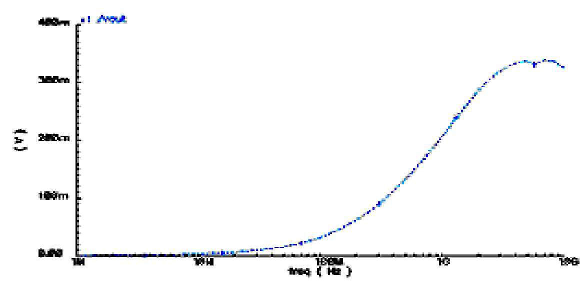

Fig. 8. Frequency response of high pass filter

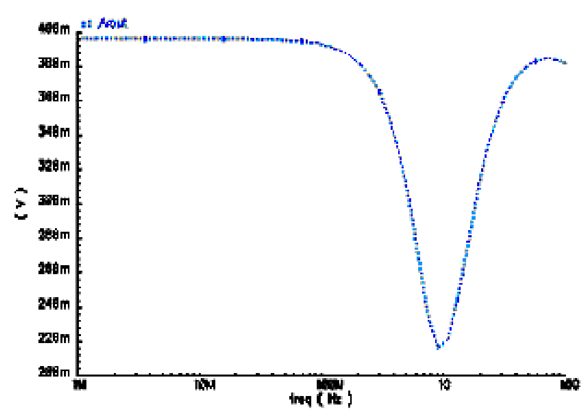

Fig. 9. Frequency response of band stop filter

4. CONCLUSION

Reconfigurable oscillator and filter are designed and simulated. It shows the oscillation frequency can be tuned in a wider range with a switching matrix that can accommodate both parallel and series connections. On the other hand, the four basic kinds of filters can be implemented with a set of inductors and capacitors, as well as a switching network. However, the performance of the filter is not very satisfactory, and it can be improved by using higher order filters. In such an approach, there is no extra digit in the control word, and one can just add more sections in the filter. On the other hand, the transistor size can be further optimized, so that the parasitic resistance is reduced, and the parasitic capacitance is under control at the same time. The simple design presented in this paper shows the possibility to make full use of the passive components, which occupy large chip area.

5. REFERENCES

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