IMPACT OF THE SCA ON HDR WAVEFORM MODELING & DESIGN

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ABSTRACT

System designers building their waveform components with the goal to address the portability and flexibility features of the SCA have simultaneously to cope with two opposite topics: the real time requirements of their applications and the middleware behavior which exhibits transport overhead and reduced determinism (higher jitter, latency). This paper present an innovative "asynchronous" design approach, currently experimented by Thales Communications S.A. inside the "Software Radio Architecture" program through the design of an SCA compliant FM3TR waveform, and put this activity in perspective for the development of new High Data Rate waveform exhibiting IP networking features.

1. INTRODUCTION

The primary goal of the Software Communications Architecture (SCA) [1] is to define an architectural framework enabling waveform portability between various Software Defined Radio (SDR) platforms and SDR reconfigurability in front several waveforms (Figure 1).

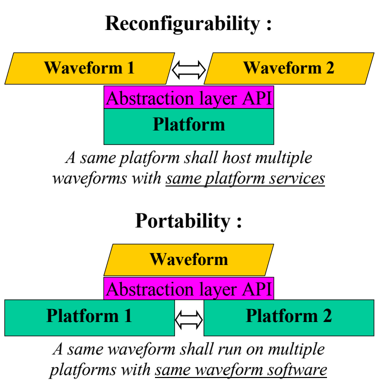

Figure 1 SDR Reconfigurability / Portability

To achieve this goal, the SCA promotes a component based design approach and defines a set of rules and interfaces to split waveform applications in components and to deploy them on a standard Operating Environment (OE) (Figure 2).

Application Programming Interfaces (APIs) are identified into the SCA as Service Definition & Transfer Mechanism (Figure 3).

Service Definition [2] provides generic interface definition between waveform components or between waveform components and platform services (Logical Devices). Service Definition guarantees components can communicate together regardless of OE or programming language.

Transfer Mechanism provides well-defined behavior when accessing local or remote services, a process where SCA OE and the SDR platform hardware resources (Processors, Communication buses,…) are mainly involved in. SCA OE is therefore essential for portability of applications and interchangeability of devices.

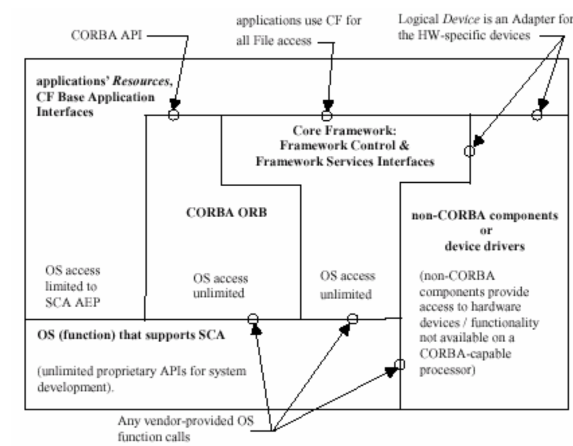

Figure 2 SCA Operating Environment (OE)

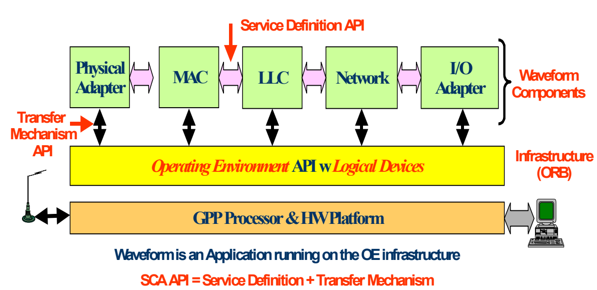

Figure 3 SCA API Definition

However, the SCA recommends a CORBA based transfer mechanism which provide inherent latency and could impact waveform performances.

To cope with this challenge, Thales Communications S.A. has initiated research effort on this topic, supported by the "Software Radio Architecture" PEA (Plan d'Etude Amont) under contract of the French MoD (DGA - Délégation Générale de l'Armement).

2. SERVICE DEFINITION

Inside the SCA, waveforms consist of one to many specific components connected in series in an OSI type stack: Physical, Media Access Control (MAC), Logical link Control (LLC), Network, I/O (Figure 3). To provide flexibility to the designer, the SCA allow a layer to be hidden so that only a higher layer is exposed.

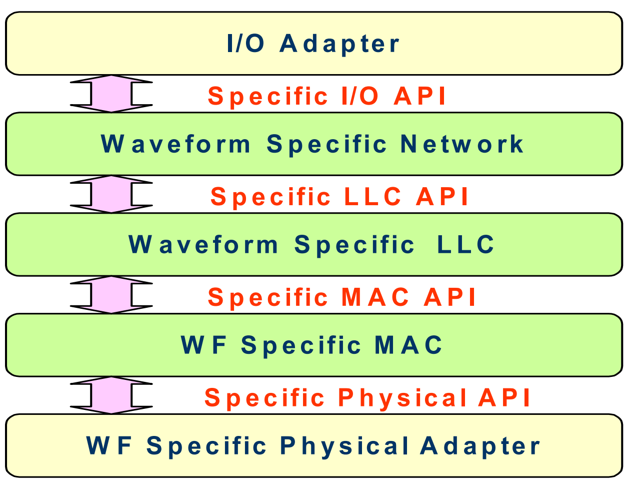

Figure 4 SCA Waveform Specific API

It could be noted that SCA does not define API for Network protocol (OSI layer 3), neither transport layer (OSI layer 4) which rely on standard API like Internet Protocol (IP) and Socket.

In this model, each component provides services to the layer above through a "Service Definition", and as such is defined as a "Service Provider", the user of these services being named the "Service User".

The Service Definition is an agreement between two components which characterizes the behavior on:

- The language & semantics used to communicate.
- How components are accessed (methods).
- What the messages parameters are (arguments).
- What the messages parameters representation are (structures, types, format).

SCA defines the fundamental "Packet Building Block (BB)" that provides for real-time data flow between all layers. The "Packet BB" has a method call "PushPacket" to send data between waveform components. Other methods in this call refer to control flow. Using the "Packet BB" in all APIs fosters common method of passing data & flow control.

3. TRANSPORT MECHANISM API

SCA promotes Transport Mechanisms based on CORBA, providing the waveform application components to be distributed in different address spaces or processors.

However, CORBA communication call through TCP/IP or UDP/IP, provides latency. Moreover, latency variance could occur, which can be as critical in real-time systems as average latency because of its impacts on predictability and system behavior.

Obviously, local (same processor) CORBA method invocations are faster than remote (different processors) method invocations.

Such behavior, especially in the remote case, may affect waveform characteristics, in particular for high demanding applications such High Data Rate (HDR) waveforms, and request innovative design approach to cope with.

4. SYNCHRONOUS VS. ASYNCHRONOUS DESIGN

A traditional "synchronous" radio design architecture is based on a strong centralized synchronization unit in charge of sequencing all the operations inside the radio (Figure 5) . This approach, well fitted for "legacy" waveforms with strong "hardware related" features, demands few processors, provides an "optimized" design, but exhibits strong dependencies between platform and waveform, preventing migration towards the SDR paradigm.

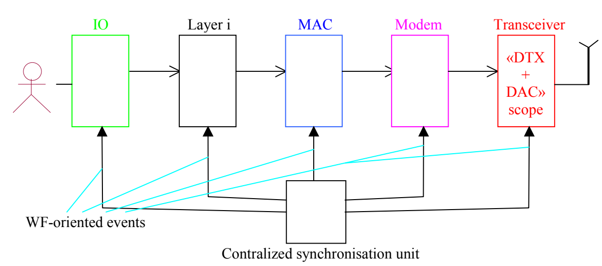

Figure 5 "Synchronous" Design Approach

The development of the SDR paradigm pushes ahead a new "asynchronous" design approach (Figure 6). In this model, each layer processes the received bulk of data at its own rate and the use of appropriate timing constraints is flexible in front of the waveform layers: very tight at the Physical layer, looser at the Network layer. For example, timing references are still needed mainly at MAC / Physical layers to manage Time Division Multiple Access (TDMA) or Code Division Multiple Access (CDMA) channel access techniques.

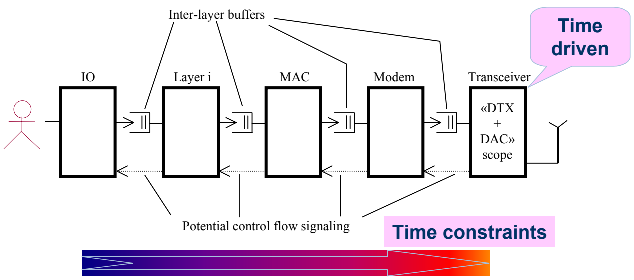

Figure 6 "Asynchronous" Design Approach

The "asynchronous" design provides the following benefits:
- Eases technological insertion.
- Takes profit of the distributed architecture.
- Looses coupling between layers.
- Leverages waveform portability.

However, the "asynchronous" design approach need to be carefully checked with legacy waveforms, when strong dependencies could continue to exist with SDR platform resources, and in respect to worst cases that become more difficult to analyze.

5. VALIDATING AN ASYNCHRONOUS DESIGN

In the scope of the French MoD (DGA) Software Architecture Program, Thales Communications S.A. is validating the "asynchronous" design approach through the development of an SCA compliant FM3TR waveform.

The FM3TR waveform exhibits to the following features:
- Open specification available [3].
- Voice and data communication capabilities.
- Fast frequency hopping (@2000 hops/s).
- Reference design available to perform interoperability tests (as the Multiband Multirole Radio – Advanced Demonstrator Model (MMR-ADM) developed by a French and German MoD cooperative program).

In front of the SCA OSI stack model, Table 1 summarizes the various layers and components which compose the FM3TR waveform, and identifies on which type of processor (General Purpose Processor (GPP) and Digital Signal Processor (DSP)) these components are running onto.

SCA OSI Layer	Component	Processor
Physical layer	Modem	Modem DSP
MAC Layer	Black MAC	Black GPP
	Red MAC	Red GPP
I/O Layer	Audio	Audio DSP
	Digital I/O	Red GPP
Management	Management	Control GPP
	GUI	IHM

Table 1 FM3TR SCA Components

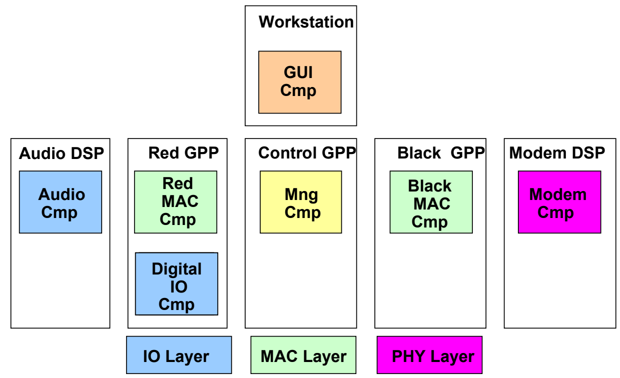

Figure 7 Mapping of FM3TR Components

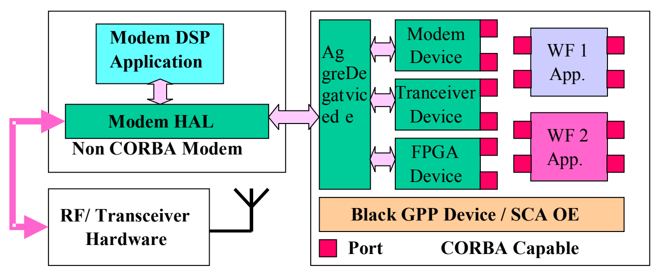

Figure 8 Thales SDR Platform Architecture (Modem)

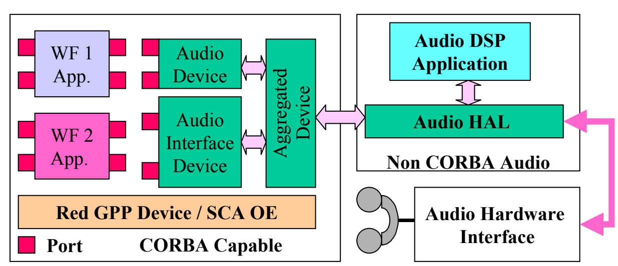

Figure 9 Thales SDR Platform Architecture (Audio)

Figure 7 maps the FM3TR components onto the Thales Communications S.A. SDR platform which exhibits the following characteristics (Figures 8 & 9):
- Black, Red & Control GPP implement SCA 2.2 compliant OE.
- Modem & Audio DSP implement an Hardware Abstraction Layer (HAL)[4] [5] [6] featuring higher

level of abstraction and component portability than in the recently published SCA 3.0 Specialized Hardware Supplement (SHS) [7].

Description of the FM3TR components is given below:

- Modem component: Performs the modulation of the data frames and demodulation of the samples flow. It ensures the detection and tracking of the waveform synchronization pattern.
- Black MAC component: Encompasses all operations necessary to adapt the incoming Red MAC data flow to the data frames manipulated by the Modem (and vice versa for reception case). This component manages frequency hopping, the waveform protocol sequencing and the waveform states.
- Red MAC component : Manages the routing of the data flow from the appropriate interface: voice or data.
- Audio component: Perform voice coding / decoding operations and manages the Audio interface.
- Digital I/O component: Performs data multiplexing / de-multiplexing to the Red MAC component and data flow control with a Data Terminal Equipment (DTE).
- Management Component: This component is an "assembly controller" which interacts with the GUI and controls all the waveform components.
- GUI component: Provides the interfaces with the user to configure the waveform parameters and monitor the waveform operations.

Voice & data flow communications exhibit asynchronous behavior between the various components (Figure 10).

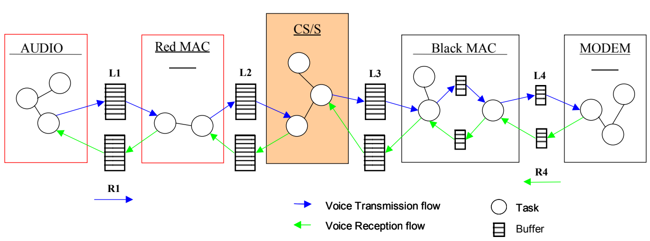

Figure 10 FM3TR Voice & Data Asynchronous Flow

In front of available flow rates, initial calculation of buffer size are identified to allow reliable asynchronous exchange of information between the components (Tables 2 & 3). Flexible implementation is done to enable buffer size adjustment in front of SDR platform characteristics.

Out-of-band overflow and underflow control mechanisms are implemented in voice & data modes to manage the asynchronous behavior. Simplified example of overflow control mechanism is given for voice transmission and the operations are as follow (Figure 11).

During operations, if an overflow is detected by the Modem component, it has to be controlled at the Black MAC component level. Upon reception of the "Overflow" control message coming from the Modem, the Black MAC slows down the transmission of voice frames to the Modem and forwards if necessary the control message to the Red MAC component. The transmission of voice data towards the Modem is resumed upon reception of the "End overflow" control message coming from the Modem.

Mode	Flow	Buffer size (bytes)			
		L1	L2	L3	L4
TW#1b @500 Hops/s	Voice Tx	60	60	60	60
	Voice Rx	60	60	60	60
	Data Tx	60	60	60	60
	Data Rx	60	60	60	60

Table 2 FM3TR Buffer Size

Mode	Flow	Flow rate (bytes/ms)		Flow rate (kbits/s)	
		R1	R4	R1	R4
TW#1b @500 Hops/s	Voice Tx	20/10		16	
	Voice Rx		20/10		16
	Data Tx	20/10		16	
	Data Rx		20/10		16

Table 3 FM3TR Flow Rate

6. IMPACT ON EMERGENT HDR WAVEFORMS

Emergent High Data Rate (HDR) waveforms are currently defined to provide Mobile Tactical Internet (MTI) networking capabilities for terrestrial, maritime and airborne applications, supporting a broad range of multimedia (data, voice and video) services.

Typical characteristics of HDR waveforms are as follow:

- Ad-hoc sub-networking.
- Adaptive routing.
- Adaptive data rate.
- Adaptive Media Access Control (MAC).
- Multiple Quality of Services (QoS).
- Dynamic RF bandwidth management.

Generic architecture of HDR waveform provides both sub-networking operations with embedded router inside the waveform and inter-networks operations based on a standard Internet Protocol (IP) layer. Generic architecture of HDR waveform encompasses the following layers (Table 4).

In comparison with a "simple" waveform like FM3TR, HDR waveforms exhibit supplementary layers like CL, LLC

& RLC which performs operations at “IP Packets” level, enabling IP transmission on the unreliable RF media through a series of transformations like segmentation for frame length adaptation to media access scheme, smart scheduling for QoS, and hop by hop acknowledgement (ACK) for link reliability.

Layer	Functions
Convergence (CL)	IP Adaptation
Radio Sub-Network (RSN)	Sub-network Routing
Logical Link Control (LLC)	Segmentation / QoS /ACK
Media Access Control (MAC)	TDMA, CDMA
Physical	Modem

Table 4 HDR Waveform Layers

From a design perspective, the “upper layer operations” (CL, RLC, LLC) are mainly scheduled on the rhythm of delivery of “IP Packet” and are therefore well adapted to support an “asynchronous” design. In contrary, the “lower layer operations” (MAC, Physical) are mainly scheduled on the rhythm of “digital samples” exchanged with the transceiver and “frames” generated at MAC level to share the access to the media (TDMA, CDMA,…). Therefore, these features provides more time constrained operations.

Interfaces between “upper layer” and “lower layer” operations lie at segmentation / re-assembly and QoS queuing, a place where it is possible to manage easily the differences of behavior between the two areas.

Taking in mind these features, it appears that future HDR waveforms defined for the MTI could be designed and implemented in a portable manner, following the SCA rules and exhibiting APIs in line with the SCA waveform breakdown structure.

This approach will lead to a more flexible approach in implementing these new waveforms and will provide benefits in term of incremental approach.

6. CONCLUSIONS

In the scope of the French MoD (DGA) “Software Architecture Program”, Thales Communications is designing the FM3TR waveform in an “asynchronous” way, to cope in an efficient manner with the inherent latency and jitter featured by CORBA transport mechanisms.

Such experimentation paves the way to develop an SCA compliant HDR waveform for MTI which exhibits upper networking layers (CL, RLC, LLC) enabling IP Packet scheduling and operations on RF media, inherently able to support an “asynchronous” design and requesting innovative design for a flexible and incremental design approach.

7. REFERENCES

[1] -Software Communications Architecture Specification, V2.2, dated 17 November 2001.

[2] - Applications Program Interface Supplement to the SCA, V1.1 dated 17 November 2001.

[3] - FM3TR (Future Multi-band Multi-waveform Modular Tactical Radio) -Test Waveform Specifications, Issue 2.0.

[4] – Software Radio Architecture & Waveform Portability – SDR’03 Conference – November 2003 - Orlando – Ref SDR’03 SW-1-003 - Christian Serra, Eric Nicollet, Serge Martin - Thales Communications S.A.

[5] – Thales Communications S.A contribution to SDR Forum HAL RFI – April 2004 - Definition of Signal Processing Subsystem (SPS) Hardware Abstraction Layer (HAL) – Christian Serra – Eric Nicollet.

[6] – SDR Forum Report on Results of RFI – SDRF-04-I-0072-V0.00 – p37 - Definition of Signal Processing Subsystem (SPS) Hardware Abstraction Layer (HAL).

[7] – Software Communications Architecture Specification, V3.0 – Specialized Hardware Supplement (SHS), dated 27 August 2004.

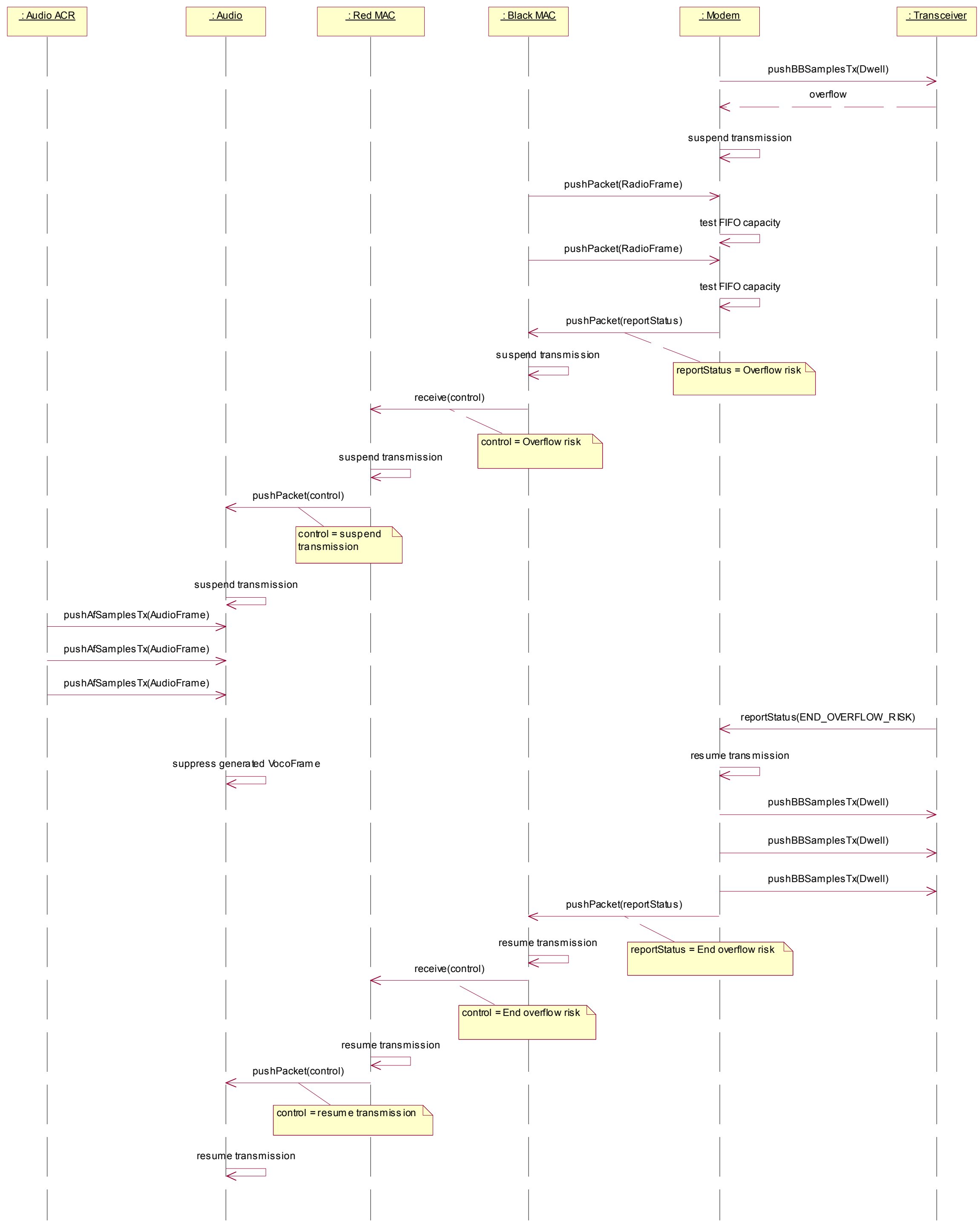

Figure 11 FM3TR Voice Overflow Management