AUTOMATED SYNTHESIS TOOLS FOR ANALOG & RF IC SOFTWARE DEFINABLE TRANSCEIVERS

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ABSTRACT

In this work, the state-of-the-art RF synthesis tools for non-linear RF and analog integrated circuits are discussed. Several commercial tools are compared and presented. For RF and non-linear analog circuits, due to the non-linearity of the circuit, design optimization is not a trivial task. This paper will give an overview of the synthesis tools for RF and Analog IC, with emphasis on trade-offs in terms of noise and distortion.

1. INTRODUCTION

The rapid grow of wireless communications has increased the need for high performance and low cost RF and analog solutions. Despite the advances in EDA (Electronic Design Automation) tools, the design and implementation of analog RF circuits relies heavily on various trade-offs and most IC design strategies depends on the knowledge and the expertise of the designers. In the past two decades, limited design tools have been developed to automate the design process. However, in RF and Analog circuits, given the various trade-offs, the design optimization is not a trivial task. Furthermore, for Software Definable Radios, where the system has to operate in multiple modes, the trade-offs in terms of Gain, Trans-conductance Gm, Current, Noise Figure, Distortion, BER, Signal-to-Noise ratio, and linearity is non-trivial.

2. BASICS OF AUTOMATIC CIRCUIT DESIGN

In this work, the state-of-the-arts automatic IC synthesis tools are reviewed and main challenges are discussed. The design steps of a typical automated transceiver synthesis tool can be summarized as follows:

1. Block Level Design: At this level of abstraction, the system issues are analyzed at the block level. For RF blocks, given that the circuit is operating at high frequency, various system parameters are approximated, and higher order distortions are often neglected. We will present a new non iterative nonlinear system solver and a new set of coordinates (Cross-References Coordinates, or CRC) that will increase the simulation accuracy while reducing the simulation time.
2. Circuit Topology Selection: For any given spec, there are various circuit topologies that must be examined. For example, there are various methods for the design of LNA, using common source/emitter, Emitter degeneration, cascade topologies, common base/gate, etc. Each topology will have a large space of design apparatus to operate in order to meet the design spec in terms of matching, gain, input/output impedance, etc. Normally the selection of the circuit topologies from the library provided by the software.
3. Circuit Level Design: The selection of the proper circuit parameters (i. e. device sizes, biasing, lumped component values) that satisfy the design goals. There are two approaches that claim partial solutions for the automatic circuit design challenge. The first one is based on iterative optimization techniques with direct device level simulation of the circuits. AMGIE [1] is an analog synthesis environment that implements a top-down hierarchical refinement design strategy for analog designs and covers the design path from specifications over the topology selection and optimum circuit sizing down to automated layout generation followed by automatic verification and datasheet extraction. The second set of techniques utilizes nature-inspired algorithms like GA (Genetic Algorithms) and EC (Evolutionary Computation) to find the optimum circuit parameters. For instance, [2] applies EC

to implement analog blocks including op-amps. The dependency of these methods to the large training database makes them inferior to the methods belong to the first approach.

4. IC Design Sensitivity Analysis and Its Effect on the System Level Blocks: Verification of the sensitivity of the block to the process variations and repeat of the above steps if necessary. This is an iterative process that needs to be imbedded in the automated design process. This step will be done pre and post layout to compare and analyze the system parameters sensitivity with respect to the circuit component variations. This is an essential tool for SDR given that any variation in the circuit parameters, will impact multiple systems. The goal of a performance-driven tool is layout of the RF circuit such that the performance degradation caused by layout parasitic remains within the specification margins imposed by the designer. For a given set of circuit specifications, several valid solutions can be found. In [3], they propose an algorithm that selects the solution that additionally maximizes the yield and the testability of the resulting layout. In the proposed approach of [4], performance specifications are translated into lower-level bounds on parasitic or geometric parameters, using sensitivity analysis. The main challenge in development of these tools is to minimize the performance degradation caused by layout parasitic.

3. REVIEW OF AUTOMATIC CIRCUIT DESIGN TOOLS

In some tools, the design knowledge captured and hard-coded in expert-system-like structures such as design plans or rules[10]. Fast methods based on simplified symbolic equations are more accurate for linear systems [11]. GPCAD is an example of these fast methods [11]. An overview of the state-of-the arts as of 1996 is provided in [7]. In this section, some of these tools are reviewed.

IDAC [10] is a design system which is able to design transconductance amplifiers, operational amplifiers, low-noise BIMOS amplifiers, voltage and current references, quartz oscillators, comparators, and oversampled A/D converters including their digital decimation filter starting from building-block and technology specifications. This design system, called Interactive Design for Analog Circuits (IDAC), is able to size a library of analog schematics (actually more than 40) as a function of technology (p-well and n-well CMOS) and desired building-block specifications. IDAC also generates a complete data sheet, an input file for SPICE2, and an input file for the analog layout program ILAC.

GPCAD [11] is a tool based on the fact that in some cases, the performance measures can be formulated as polynomial functions of the design variables. As a result, amplifier design problems can be formulated as a geometric program, a special type of convex optimization problem for which very efficient global optimization methods have recently been developed. The synthesis method is therefore fast, and determines the globally optimal design; in particular the final solution is completely independent of the starting point (which can even be infeasible), and infeasible specifications are unambiguously detected.

AMGIE [1] is a synthesis environment for analog integrated circuits that is able to increase design and layout productivity for analog blocks. The system covers the complete design flow from specification over topology selection and optimal circuit sizing down to automatic layout generation and performance characterization. It follows a hierarchical refinement strategy for more complex cells and is process independent. The sizing is based on an improved equation-based optimization approach, where the circuit behavior is characterized by declarative models that are then converted in a sequential design plan. Supporting tools have been developed to reduce the total effort to set up a new circuit topology in the system's database. The performance-driven layout generation tool guarantees layouts that satisfy all performance constraints. Redesign support is included in the design flow management to perform backtracking in case of design problems.

ISAAC [15] (interactive symbolic analysis of analog circuits) derives all AC characteristics for any analog integrated circuit (time-continuous and switched-capacitor, CMOS, JFET, and bipolar) as symbolic expressions in the circuit parameters. This yields analytic formulas for transfer functions, CMRR (common-mode rejection ratio), PSRR (power-supply rejection ratio), impedances, noise, etc. Two novel features are included in the program. First, the expressions can be simplified with a heuristic criterion based on the magnitudes of the elements. This yields interpretable formulas showing only the dominant terms. Second, the explicit representation of mismatch terms allows the accurate calculation of second-order effects, such as the PSRR. ISAAC provides analog designers with more insight into the circuit behavior than do numerical simulators and is a useful tool for instruction or designer assistance. Moreover, it generates complete analytic AC circuit models, which are used for automatic sizing in a nonfixed topology analog module generator.

MAELSTROM [20] is an approach that synthesizes a circuit using the same simulation environment created to validate the circuit. They introduce a novel genetic/annealing optimizer, and leverage network parallelism to achieve efficient simulator-in-the-loop analog synthesis

OASYS [17] is a hierarchically structured framework for analog circuit synthesis. This hierarchical structure has two important features: it decomposes the design task into a sequence of smaller tasks with uniform structure, and it simplifies the reuse of design knowledge. Mechanisms are described that select from among alternate design styles and translate performance specifications from one level in the hierarchy to the next lower, more concrete level. A prototype implementation, OASYS, synthesizes sized transistor schematics for CMOS operational amplifiers from performance specifications and process parameters. Measurements from detailed circuit simulation and from actual fabricated analog ICs based on OASYS-synthesized designs demonstrate that OASYS is capable of synthesizing functional circuits.

ANACONDA [26] is based on a new numerical search algorithm efficient enough to allow full circuit simulation of each circuit candidate, and robust enough to find good solutions for difficult circuits. Comparison of synthesized circuits against manual industrial designs demonstrates the utility of the approach.

BLADES [12] uses both formal and intuitive knowledge in the design process. A prototype design environment, BLADES, which uses a divide and conquer solution strategy, has been successfully implemented and is currently capable of designing a wide range of subcircuit functional blocks as well as a limited class of integrated bipolar operational amplifiers. BLADES is believed to be the first successful design expert system in the analog design domain. It uses different levels of abstraction depending on the complexity of the design task under consideration. The importance of the abstraction level lies in the fact that once design primitives are defined, the problem of extracting the knowledge (design rules) become less complex.

3. CRC BASED SIMULATION

One of the main challenges in the development of RF and analog circuits is the non-linearity of the circuit resulting in limited dynamic range, inter-modulation, and harmonic distortion of the signal. Given that the circuit is operating at high frequency and has several poles with slow and fast time-constant, the steady state simulation of the circuit to examine the IM products, harmonics, and non-linearity effects, is still a challenging issue. This problem has been partially resolved using Harmonic Balance method; however, the simulation results have their limitations. In this work, a novel non-linearity modeling method, termed "Cross-Referenced Coordinates" (CRC) is introduced [37-39]. The CRC model uses multi-dimensional pass-band to base-band mapping of each signal and its harmonics and IM products resulting in increase in simulation efficiency and more accuracy when compared to the other methods. It will be shown that for digital modulation, where the ratio of the bandwidth of the signal to the carrier frequency is small, the CRC is highly accurate and offers better time efficiency. A complete general purpose C++ toolbox has been implemented based on this new technique.

4. CONCLUSIONS

Several commercial tools are compared and presented. There are still many challenges ahead of RF and Analog synthesis tools to make them as mature as digital synthesis ones. The references provided in section 5 can be used as a reference jump start. [1,2,5-33] discussing various techniques for analog synthesis. [34-35] are mainly layout synthesis tools.

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