PRACTICAL TRANSMIT/RECEIVE SYSTEM FOR SOFTWARE RADIO

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ABSTRACT

Digital transmitters and receivers are vital elements in any software radio system. This paper considers the practical hardware requirements of a number of typical digital modulation schemes. It deals with both the digital processing resources and the analog characteristics required of both input and output paths. Pentland Systems has recently developed a demonstration system designed to switch, under software control, between two, disparate modulation schemes. The paper describes the design of the demonstration system (including using FPGAs for DSP) outlines some of the problems encountered and their solutions. The paper ends with a discussion of the results achieved by the system.

1. INTRODUCTION

The demands placed by software-defined radio on digital receivers and transmitters are numerous and wide-ranging. Common modulation schemes used in commercial communications can vary from narrow band formats with tight filter constraints, such as GSM's GMSK, to wideband formats with multiple channels, complex coding schemes and high dynamic range requirements as demonstrated by the QPSK spread-spectrum schemes used in WCDMA. Military and proprietary systems show an even greater variation. The digital TX/RX components of a SDR system need sufficient analog performance and digital capacity to manage the different requirements placed on the system.

Pentland Systems have a developed a family of products that includes digital TX and RX suitable for SDR systems. In order to show the products' capability it has become necessary to put together a demonstration system that illustrates the salient features of a SDR. This paper discusses design considerations for the test system, outlines the solution and gives details of results achieved.

2. SYSTEM DESIGN REQUIREMENTS

2.1 General Design Requirements

The objective of this application was to design a test system that could switch between two disparate modulation schemes using only changes under software control. The system was to be used to demonstrate capability, but the primary function was to increase Pentland Systems' understanding of the design and hardware real-estate requirements of a SDR system.

2.2 Modulation schemes

The two modulation schemes used, QAM and MSK, were chosen because the formats are popular in modern communications, and have differing filtering requirements and characteristics. The formats were deliberately kept quite simple, as the aim was to demonstrate 'proof of concept' rather than spend a lot of time debugging complex modulation algorithms**.**

2.2.1 Frequency Shift Keying (FSK)

FSK is a popular modulation format used in a number of commercial applications (pagers for example). The frequency of the signal is directly changed as a function of the data bits. In its simplest form, binary phase shift keying (BFSK) '1' and '0' are represented by two frequencies (f_1 and f_2). The output from a BFSK

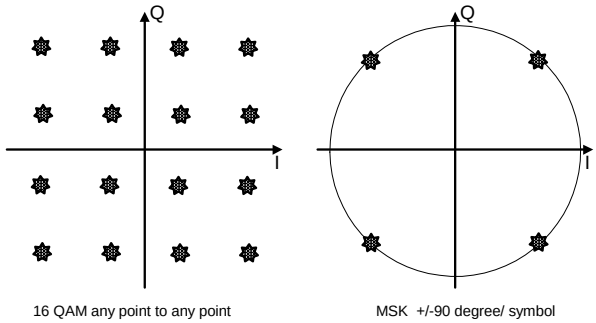

Figure 1 QAM/MSK Constellations

modulator is a constant amplitude signal that varies between these two frequencies. A specific form of FSK known as Minimum Shift Keying (MSK) is of particular interest in digital I/Q demodulators. A frequency shift from a nominal center frequency gives rise to advancing or retarding phase. Because of the orthogonal nature of the signal, phase shifts of (2N + 1) π/2 radians per symbol are easily detected within an *I/Q* demodulator. The minimum phase shift to produce such a signal is +/-π/2 radians (or 90°) per symbol. If the frequency change occasioned by a '1' or zero is chosen to cause a 90° phase shift this is known as MSK modulation. [1] In order to achieve MSK the difference between f_1 and f_2 must be equal to half the bit rate.

The constant amplitude of this format means that the dynamic range requirements in the TX and RX are low. However with phase detection being the means of demodulation the frequency accuracy of the transmitter needs to be high. GSM cellular phones, which use a form of MSK, require a frequency accuracy of 0.1ppm.

2.2.2 Quadrature Amplitude Modulation (QAM)

If greater spectrum efficiency is required it is necessary to move away from constant amplitude schemes and use both amplitude and phase to convey information. N-QAM is a modulation type prevalent in modern digital communication systems. In this format the bits are mapped to N symbols in the IQ plane. For example in 16-QAM the bits are mapped to four I values and four Q values giving 16 possible states. As 16 is 2^4, four bits are mapped into each symbol.

This type of signal, whilst allowing a greater number of bits per symbol to be transmitted, is more vulnerable to noise and demands a greater dynamic range from both transmitter and receiver. The symbol mapping becomes more complex as N increases, Grey coding is often required to reduce the effect of bit errors and, as the demodulation requires clock recovery, scrambling of the data may also be necessary to avoid long runs of '1' or zeroes. All this adds to the complexity of the DSP. The amplitude modulation calls for a greater dynamic range in both sides of the transceiver. As N increases so does the system's susceptibility to noise and phase error. It is important that the TX and RX achieve good quadrature balance. Clock phase recovery is important in the receiver circuitry.

Figure 1 shows an I/Q (constellation) diagrams for 16-QAM and MSK demonstrating their relative complexities.

2.3 System Components

The demonstration system has three basic components consisting of a digital receiver and digital transmitter both mounted on an embedded processor card. Overall control over parameters and display of results is handled by a laptop PC.

2.3.1 Digital Receiver

Figure 2 shows a simplified block diagram of Pentland Systems, RAD-2 digital receiver. Designed to meet the requirements of software radio applications three main principles were adhered to in its design [2] that is it the receiver should be:

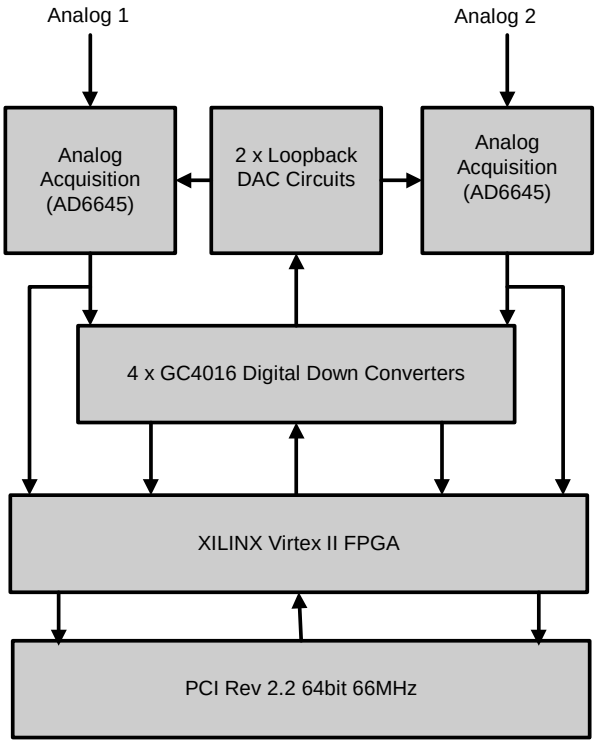

Figure 2 RAD-2 Digital Receiver

Reconfigureable: An on-board FPGA, reprogrammable over the PMC's JTAG interface allows the receiver to be re-formatted without its removal from the system.

Flexible: Wide input bandwidth and high dynamic range of analog front-end makes it suitable for a number of applications. High speed ADC (up to 105MHz) allows signals up to 50MHz to be directly digitized without down converting to an IF. [3]

Modular: The PMC format is a good starting point for this, as its standard interface allows the units to be switched in and out easily. In addition the system is readily scaleable by the adding of additional modules.

The PMC format has the added advantage of being able to be sited on numerous embedded processors or FPGA baseboards available in the VME format.

2.3.2 Digital Transmitter

Figure 3 shows a simplified block diagram of Pentland Systems' RAD-T2 Digital Transmitter. Also designed with SDR as one of its target applications the same design principles adhered to in the RAD-2 are reflected here: Large FPGA resources give a considerable measure of reconfiguration capacity. A broadband output and 14bit digital to analog conversion provides a >80dB dynamic range suitable for many modulation formats.

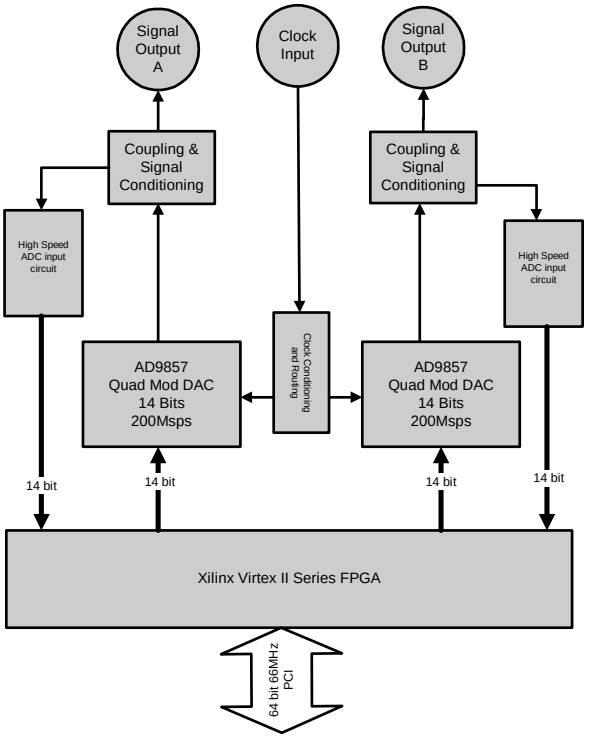

Figure 3 RAD-T2 Digital Transmitter

Using a Quadrature modulating DAC instead of a straight DAC allows for flexibility in choice of modulation schemes. The modular PMC format provides a scaleable, standardized interface.

2.3.3 Embedded Processor

There are numerous embedded processors, capable of running DSP algorithms, available in VME format. This system used Dy4's CHAMP AVII Quad Power PC card, primarily because Pentland Systems are familiar with the product and having used it before no additional time was required to get the PMC (VxWorks) device drivers integrated into its OS.

3. SYSTEM DESIGN

3.1 Design Partitioning

One of the first tasks involved the partitioning of the design. Specifically how the DSP should be distributed between the FPGA resources available and the embedded processor. This is usually a speed/flexibility trade–off. With high clocking rates, increasing gate sizes and ability to be reprogrammed in situ, the FPGA is starting to cover many of the application traditionally confined to DSP processors. In general FPGAs are best suited to parallel processing, involving high numbers of MAC operations, bit level calculations and pipelining data, DSPs are better at encoding, formatting, (de)mapping and translation the data.

In practice the decision on where to split the DSP in a given system will depend on a number of other factors:

Power: The FPGA's greater speed in DSP carries with it a power penalty. In commercial air-cooled systems this is not often a problem, but it becomes increasingly important as software radios move into battery powered and/or conduction cooled applications. These restrictions can be severe, for example: Pentland Systems' PMC modules are designed to be compliant with the conduction-cooled PMC standard which places a limit of 7W power dissipation on the cards in a conduction-cooled environment. [4] A lot of effort has gone into producing low power design of filters [5] modulators and other radio system components. These techniques are valuable, but often demand longer design cycles. If the maximum power is fixed the DSP hardware/software split is often decided by the amount of time available to optimize the FPGA hardware.

FPGA size: DSP can quickly use up available FPGA resources. For example a simple, single channel, 7-tap filter using 16-bit data and 16-bit filter weights requires, at first estimate, 1,792 (7 x 16 x 16) full adders, which may represent 20k gates. Reduction of hardware real estate has attracted a lot of effort in recent years and use

of simple DSP 'tricks' can often quickly reduce the number of gates required by an order of magnitude from the original estimates [6] However there is a fixed amount of FPGA resources available on the PMC so care must be taken to use it in an efficient manner, concentrating on repetitive algorithmic operations that require parallel processing. In the receiver this includes filtering, digital down conversion (DDC) and decimation. For the transmitter this includes filtering, digital up-conversion and up-sampling. In general the PMC resources are best use to 'condition' the digital signals either immediately prior to transmission or directly after A to D conversion. A second driver for conditioning the signal as close to the convertors is:

Data Transfer Rates: High-speed convertors produce/require high data rates; the two 105MHz ADCs on the RAD-2 digital TX are capable of producing data at the rate of 420MB/s. For efficiency, quick reduction to the minimum number of bits required for effective DSP is required. In the receiver this points to removal of extraneous bits immediately after A to D conversion, through decimation, which can be combined with filtering. Conversely up-sampling of the signal in the transmitter prior to reconstruction needs to be performed as close to D to A conversion as possible.

In this test case Pentland Systems wanted to maximize the usage of the digital TX and RX capabilities so all the modulation, demodulation, post and preconditioning of the data was implemented within the PMC devices. The potential power constraints were ignored although the final power noted. The embedded processor was used to provide to control/program the PMC devices under instruction from the laptop.

3.2 The Test System

Figure 4 show the demonstration set-up with the digital RX and TX mounted on the PMC sites of a 6U VME processor. The modulated signal generated by the digital TX is passed directly to the RX where it is demodulated. The overall control of the system is via a laptop through which the operator can select modulation type, data patterns, data rates, and output frequencies. The output from the digital receiver is also displayed on the laptop.

3.1.1 Modulation

QAM: The demonstrator makes use of the inherent capabilities of the Quadrature Modulating DAC to provide the quadrature modulation, filtering, up-sampling and digital up-conversion (DUC) from baseband. [7] The FPGA resources are used to supply conditioned, 14-bit, interleaved I and Q test data at baseband. The systems

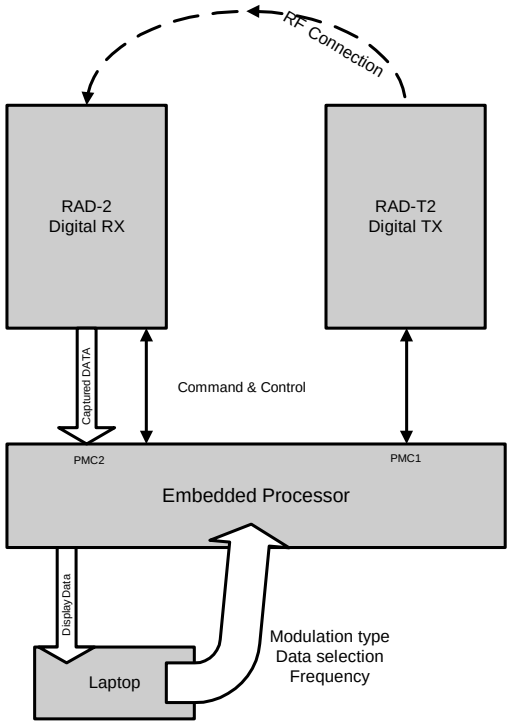

Figure 4 Test System Block diagram

66MHz clock is used to derive digitizing and symbol rate clocks. Symbol mapping gray coding and scrambling delegated to embedded DSP. In this case in order to avoid unnecessary complication the test data streams (PRBS, known fixed patterns or sine waves) were generated on board the PMC with the embedded processor providing control signals. The dynamic range provided by the 14-bit DAC is sufficient for delivery of the QAM signal

FSK (MSK): FSK modulation is achieved by directly modulating the DDS of the quadrature modulator. Two frequency states are preset into the device the selection bus is then directly driven by the ones and zeros of the data stream, causing the internal NCO to toggle between the two frequencies. [8] MSK is achieved by selecting the two pre-set frequencies so that the difference is one-half the data rate. The pre-set frequencies can be modulated at up to 10MHz and an output frequency of up to 80MHz is achievable. This configuration represents an uncomplicated FSK modulation, as only simple filtering of the data is available. A better (MSK) modulation can be achieved by using the quadrature modulator. This can be implemented by changing the bit to symbol mapping in the test signals. Further, the filter taps can be changed to produce Gaussian filtering allowing the popular GMSK format (used by the GSM networks) to be transmitted.

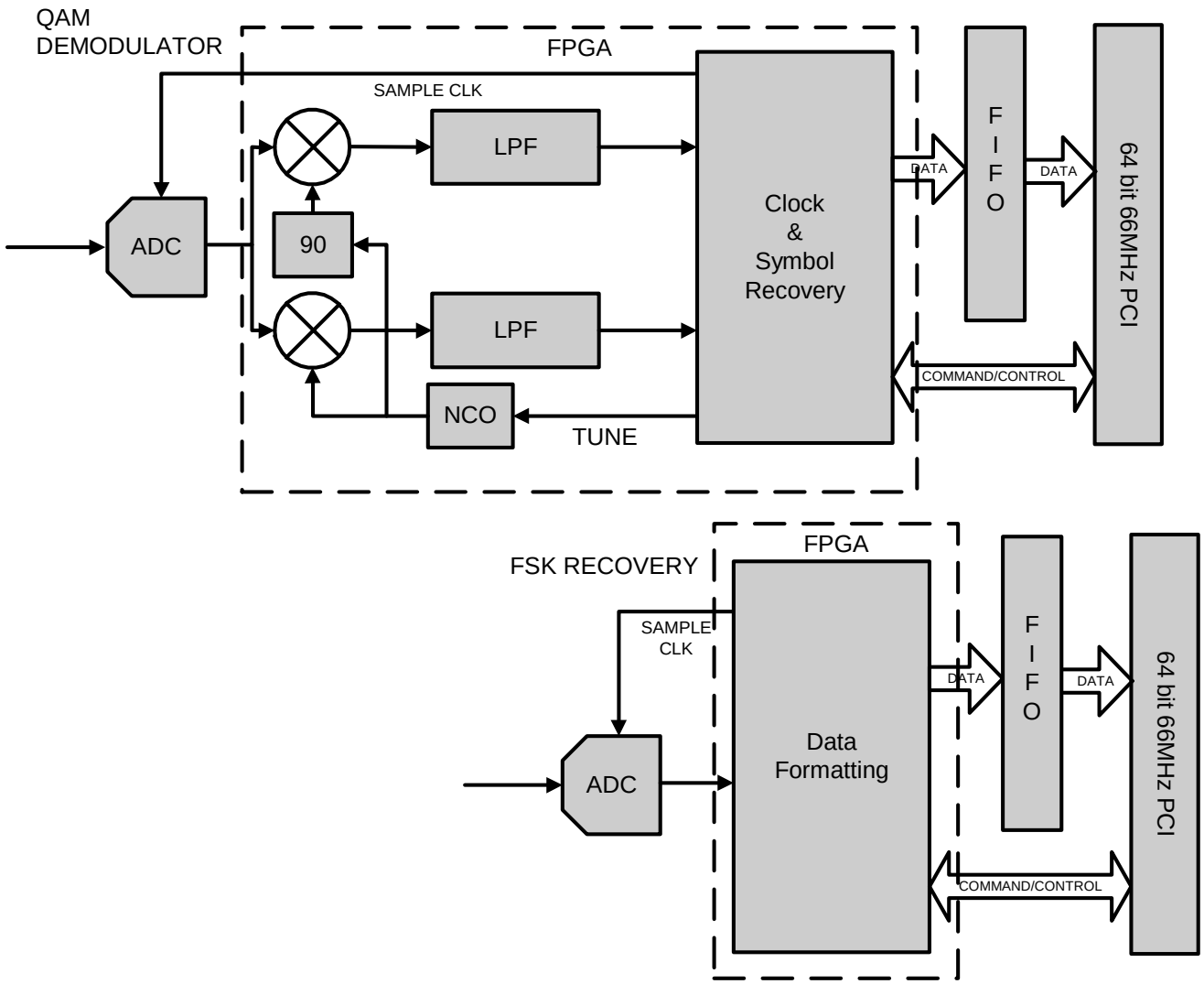

Figure 5 Demodulator Block Diagrams

The NCO provides high frequency accuracy; frequency stability is related to overall stability of the sampling clock. In this case the 66MHz PCI system clock was used to derive these frequencies.

3.1.2 Demodulation

QAM: The system uses a standard quadrature demodulator circuit to take the data stream down to symbols – digitized symbol are demapped in the FPGA, the data then transferred to PC via embedded processor where FFT software used to analyze the output. The dynamic range provided by the 14-bit ADC is sufficient for complete recovery of the QAM signals

FSK: For the MSK (90° phase shift per symbol) example it would be possible to use same IQ demodulator as for QAM example. The orthogonal nature of the signals makes them easy to detect in a quadrature demodulator. In

this case a decision was made to change as much as possible between each format. As a result straight digitization is used in the case of the FSK modulated signals. The raw data transferred directly to the processor, which then formats the data for display on the PC in either time or frequency domain. The removal of DDC and decimation circuitry means that the raw data rate (of up to 420MB/s) is transferred across the PCI interface, allowing that component of the design to be tested as well.

Figure 5 shows the demodulators as implemented.

3.4.3 System Control

The control for the demonstration system is provided by a laptop connected to the embedded processor via a network crossover cable. A command line interface allows the user to set modulation type, filter coefficients, data rates, modulation frequencies (for FSK) and data patterns. Re-programming the FPGA for the different modulation types is achieved using the PMC's JTAG interface. Display returned data in frequency or time domain. In both cases transient capture the modulated inputs was used. Real-time capture is possible, but the refresh rate of FFT on PC was unable to cope – so transient capture has been used instead.

4. RESULTS

It has been possible to design a system able to switch between two disparate modulation schemes, using the resources available on the digital TX/RX PMC modules. Simplification of the mapping/encoding was necessary to complete the task in the allotted time frame. More complex operations such Gray coding and scrambling of the data that would have been relegated to embedded DSP have been ignored for this test case.

The quadrature modulation and demodulation (as expected) proved to the most power hungry of the two set-ups. This single channel, 16-bit operation, using a 66Mhz sample clock produced overall power increase of less than 2W on standard digitizing TX/RX operation. Increasing clock rate or adding more channels would add to the overall power consumption. It should be noted that the emphasis design brief was to produce a working system; lower power designs were not investigated.

Of the two systems, the largest consumption of real estate was again the quadrature demodulator, which used about 8% of a 3 Million gate FPGA. However combined with the existing data transfer control circuits this still amounts to less than 15% of the available resources.

5. CONCLUSIONS

The design considerations for a practical SDR system have been discussed the hardware/software split for the DSP and the need for signal conditioning close to the point of conversion described. It has been proposed that PMCs offer a means providing this conditioning before/after the main DSP is implemented in an embedded processor or FPGA baseboard. It has been shown that the available on board FPGA resources are clearly able to cope with these requirements, Time and effort needs to be expended in partitioning the design when higher clock rates or multiple channels are required. In a power-limited environment, greater attention would need to be paid to low power design and hence longer design cycles can be expected.

It worth noting that the complexity of design trade-offs is substantial and this prepare serves as a brief introduction to subject.

6. REFERENCES

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