AN IMPLEMENTATION OF THE SDR BASEBAND PLATFORM FOR OFDM COMMUNICATION SYSTEMS

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ABSTRACT

Orthogonal Frequency Division Modulation (OFDM) technology has been adopted by a variety of standards which include the European Telecommunications Standards Institute (ETSI) for Terrestrial TV, the IEEE 802.11a/g standard for wireless LANs operation at bit rates up to 54Mb/s and the IEEE 802.16a/d/e for wireless MANs at bit rates up to 72.61Mb/s. In this paper, the use of a digital signal processor is explored for OFDM communication systems with the goal of increasing flexibility. We discuss the hardware and software architecture of the implemented SDR baseband platform for the OFDM communication systems, considerations for re-configurability, and test results. We will also address practical issues for real-time processing and optimization schemes of DSP modem software, and provide detailed measurement results of DSP performance over the OFDM communication systems.

1. INTRODUCTION

Wireless LAN, Home Network, Digital broadcast, and the like as well as the 2G and 3G provide service users with ample convenience, but on the other hand, a wide variety of standards and protocols cause the service users a lot of confusion. Moreover, the circumstances that an individual can choose are need. In these conditions infested with data, text, image, audio, video, and so forth, a software Defined radio system that can support multi-mode and multi-standard is demanded.

The hardware needs to be designed to have open architecture so that the SDR system has flexibility to meet diverse standards now being used and developed. Analog front-end and Application Specific Integrated Circuits (ASIC) have been used to follow fixed standards in design of the existing terminals, but reconfigurable Digital Signal Processors, reconfigurable Filed Programmable Gate Arrays (FPGA), and digital types of front-ends called digital intermediate frequency converter will be used instead. The SDR systems expand the range of digital signal processing to the IF from the baseband. Moreover, the performance of Analog-to-Digital (AD), digital-to-analog (DA) converters are being improved, and on the RF side, various tunable RF circuit design methods are being suggested so that the RF part can support multi-mode and multi-band. These facts will also help commercialization of the SDR [1].

The first SDR was the Speakeasy system developed for the military purpose in the US. There have been numerous researches since then, and the military and commercial purpose products based on the SDR are being released.

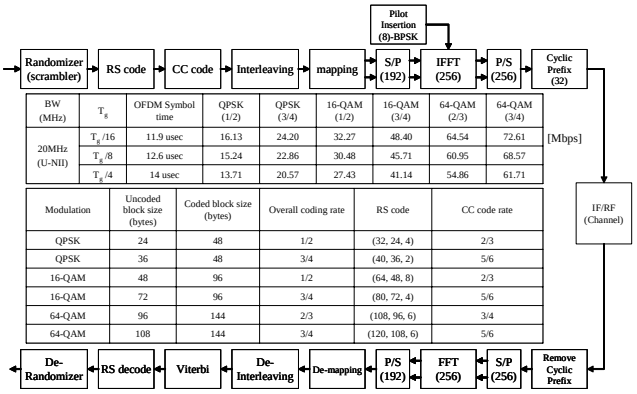
Wideband wireless OFDM communication systems have gained in popularity due to the spectral efficiency and capability of OFDM to transmit high data rates over broadband radio channels with frequency selective fading [2]. Because of its benefit, OFDM technology has been adopted by a variety of standards which include the IEEE 802.11a/g standard for wireless LANs operation at bit rates up to 54Mb/s and the IEEE 802.16a/d for wireless MAN at bit rates up to 72.61Mb/s.

In this paper, the implementation of the SDR baseband platform for OFDM communication system that is suitable for IEEE802.16a and IEEE802.11a environment is described. The rest of this paper is organized as follows. In section 2, we give description of IEEE802.16a and IEEE802.11a standard. The hardware architecture of the implemented SDR baseband platform and the software implementation are described in section 3 and section 4, respectively. In section 5, the experimental results of the implemented SDR baseband platform are justified and the concluding remarks are made in section 6.

2. SYSTEM PARAMETERS

IEEE802.16a WMAN has variable transmission data rate depending on the channel bandwidth (BW), the modulation type employed - quaternary PSK (QAM), 16-quadrature amplitude modulation (QAM) or 64-QAM , the amount of error-correcting code overhead (1/2, 2/3 or 3/4 overall coding rate) and the ratio of Cyclic Prefix (CP) time to useful time. Figure 1 shows the basic block diagram and the variable transmission data rate from 16.13Mb/s to 72.61Mb/s with 20MHz channel BW specified in

IEEE802.16a standard. An OFDM symbol consists of a useful part and a CP. Here, the useful part is generated from 192 data symbols, 56 frequency nulls and 8 pilot subcarriers. A 256 point IFFT converts the frequency domain symbol into a sequence of complex time domain samples. The baseband time domain sampling frequency is 160/7 MHz. The subcarrier frequency spacing is 89.28 kHz [3].



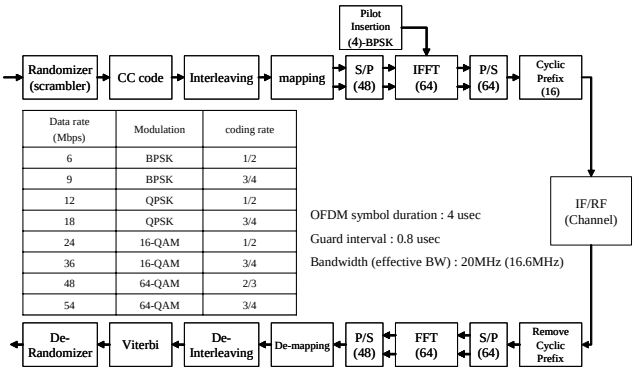
BW (MHz)	T_g	OFDM Symbol time	QPSK (1/2)	QPSK (3/4)	16-QAM (1/2)	16-QAM (3/4)	64-QAM (2/3)	64-QAM (3/4)
20MHz (U-NII)	T_g/16	11.9 usec	16.13	24.20	32.27	48.40	64.54	72.61
	T_g/8	12.6 usec	15.24	22.86	30.48	45.71	60.95	68.57
	T_g/4	14 usec	13.71	20.57	27.43	41.14	54.86	61.71

[Mbps]

Modulation	Uncoded block size (bytes)	Coded block size (bytes)	Overall coding rate	RS code	CC code rate
QPSK	24	48	1/2	(32, 24, 4)	2/3
QPSK	36	48	3/4	(40, 36, 2)	5/6
16-QAM	48	96	1/2	(64, 48, 8)	2/3
16-QAM	72	96	3/4	(80, 72, 4)	5/6
64-QAM	96	144	2/3	(108, 96, 6)	3/4
64-QAM	108	144	3/4	(120, 108, 6)	5/6

Figure 1. The functional block diagram of the IEEE802.16a

As the 5GHz WLAN standard, IEEE802.11a WLAN also has variable transmission rate from 6Mbps to 54Mbps. It utilizes a 64 point IFFT with 48 data symbols, 12 frequency nulls, and 4 pilot subcarriers. The baseband time domain sampling frequency is 20MHz and the subcarrier frequency spacing is 312.5KHz. Figure 2 shows the basic block diagram of the IEEE 802.11a WLAN and the other specific parameters [4].



Data rate (Mbps)	Modulation	coding rate
6	BPSK	1/2
9	BPSK	3/4
12	QPSK	1/2
18	QPSK	3/4
24	16-QAM	1/2
36	16-QAM	3/4
48	64-QAM	2/3
54	64-QAM	3/4

OFDM symbol duration : 4 usec
Guard interval : 0.8 usec
Bandwidth (effective BW) : 20MHz (16.6MHz)

Figure 2. The functional block diagram of the IEEE802.11a

3. HARDWARE ARCHITECTURE OF THE SDR BASEBAND PLATFORM

The developed SDR baseband platform consists of three Texas Instrument' TMS320C6416 fixed point DSP processors operating at the frequency of 720MHz, one Altera' EP1S40B968C6 Stratix filed programmable gate array (FPGA), two ADS5500 analog to digital converters (ADCs) for 14-bit digitization with 125 MHz, one dual digital to analog converter (DAC), DAC2904, operates up to 125 MHz with 14-bit resolution, PLX9054 for PCI interface, several memories such as Flash ROM, dual-port SRAM and external interfaces for connection to the extra DSP daughter module and to control a RF transceiver. Figure 3 shows the block diagram of the SDR baseband platform.

Considering the characteristics of the SDR baseband platform, there are the PLX9054 for the PCI interface, a 32-bit local bus, and HPI (Host Port) bus for downloading the execution code for the three DSP processors. The configuration files in the EPC16 configuration device is selected by the DSP (Tx) for re-configuring the FPGA's functionality. The processing resources of the DSP processor can be extended simply when they are in short through the external connector to the extra DSP daughter modules. The data exchanges between PCI interface and DSP processors are done through dual-port asynchronous SRAM (IDT70V657S12DR) and the data exchanges between FPGA and DSP processors are done through dual-port synchronous SRAM (ITD70V3599S133DR). Figure 4 shows the implemented SDR baseband platform.

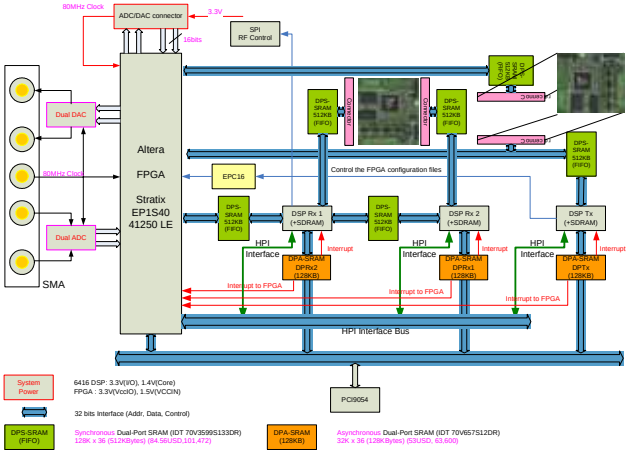


Figure 3. The block diagram of the baseband platform.

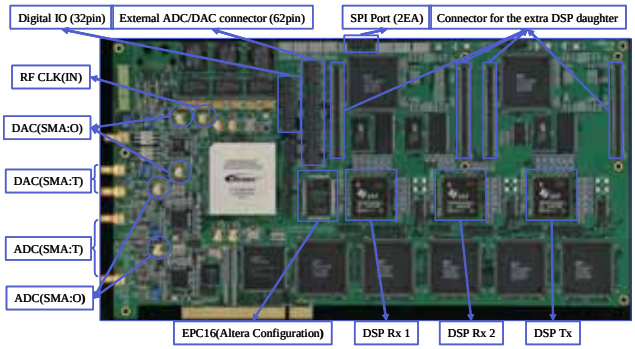


Figure 4. The block diagram of the baseband platform.

4. SOFTWARE IMPLEMENTATION

The algorithms specified in the IEEE802.16a and IEEE802.11a, including randomizer, shortened-and-punctured Reed-Solomon encoder, convolutional encoder, interleaver/de-interleaver, mapper/de-mapper, IFFT/FFT and synchronization algorithms are implemented by DSP software.

Considering the development of DSP software, DSP manufacturers provide their users with various optimization schemes for their own DSPs. Texas Instruments (TI) recommends using intrinsics to replace the complicated C code. Intrinsics are special functions that map directly to inlined instructions to optimize the C code quickly. Many instructions that are not easily expressed in C code are supported as intrinsics. TI also recommends using wider memory access for smaller data widths to maximize data throughput on the DSP and using the linear assembly code[5-7].

The TMS320C6416 DSP processor has Viterbi Decoder Coprocessor (VCP) and Turbo Decoder Coprocessor (TCP) for channel coding, which speed up decoding operation. The need procedures for decoding convolutional code are de-puncturing, branch metric calculation and EDMA configuration. The VCP is used to decode the convolutional code [8].

The shortened-and-punctured Reed-Solomon encoder and decoder are developed in linear assembly code and measured cycle counts to process are shown in Table 1[9-10].

Table 1. Measured cycle counts for shortened-and-punctured Reed-Solomon Encoding/decoding

Modulation	RS Code	Encoding Cycle Count	Decoding Cycle Count
QPSK	(32,24,4)	299	4,831
QPSK	(40,36,2)	473	4,927
16-QAM	(64,48,8)	587	4,673
16-QAM	(80,72,4)	787	4,831
64-QAM	(108,96,6)	973	4,891
64-QAM	(120,108,6)	1,071	4,891

The DSP software for the transmission and the reception is developed employing one DSP processor (DSP Tx) and two DSP processors (DSP Rx1, DSP Rx2 – indicated in Figure 2 and Figure 3) respectively. A summary of the cycle counts measured to implement the various functionality of the transceiver for processing one OFDM symbol (IEEE802.16a) is shown in Table 2.

The FPGA carries out the sampling rate conversion between the baseband time domain sampling rates of 160/7 MHz (IEEE802.16a) and 20MHz (IEEE802.11a) and ADCs/DAC sampling rate 80MHz. Figure 5 shows the functional block diagram of the FPGA and the internal resource usage is shown in Table 3.

Table 2. Measured cycle counts for processing one OFDM symbol.

Transmitter Processing (DSP Tx)	Cycle Count	Receiver Processing (DSP Rx 1)	Cycle Count
Randomizer (72 bytes)	23	Frame Detection -14 OFDM duration buffer size search	19,208
Reed Solomon Encoder (80,72,4)	787	Symbol Detection	3,376
Convolutional Encoder (coding rate: 5/6)	476	Channel Estimation	25,768
Interleaver (768 bits)	429	Remove CP (32 samples) & FFT (256 point)	1,576
16-QAM Mapper (192 data symbols)	357	Channel Compensation	744
IFFT Input data Generation (8-pilot insertion & formatting)	373	16-QAM De-Mapper (192 data symbols)	831
IFFT(256-point) & Add CP(32 samples)	2,250	Total (except synchronization – 3,151)	51,503
Total	4,695	Receiver Processing (DSP Rx 2)	-
-	-	De-Interleaver (768 bits)	429
-	-	VCP Input Generation (De-Puncturing, Branch matrix calculation)	792
-	-	Reed Solomon Decoder (80,72,4)	4,831
-	-	De-Randomizer	23
-	-	Total	6,075

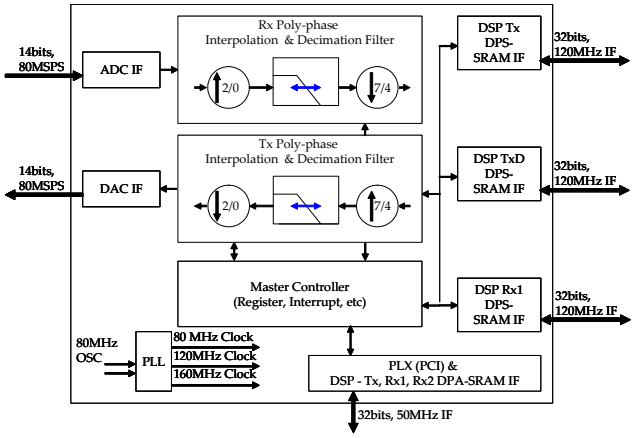


Figure 5. The functional block diagram of the FPGA

Table 3. FPGA internal resource usage

-		Usage.
Total Logic Element		13,057 (31%)
Total Pin		366 (52%)
Total Memory Bit		28,672 (< 1%)
DSP block 9-bits Element		112 (100%)
Maximum Operating Frequency	PCI Interface	104.82 MHz
	Sync. Dual-Port SRAM Interface	140.51 MHz
	FIR Filter	172.39 MHz

5. TEST RESULTS

We tested the implemented SDR baseband platform in a personal computer (PC). Its functionality is experimented by baseband loop-back connection of the transmitter and receiver at DAC-ADC. In this section, we show some measured data with IEEE802.16a software.

The preamble and power spectrum of the transmitted signal are shown in Figure 6 and Figure 7.

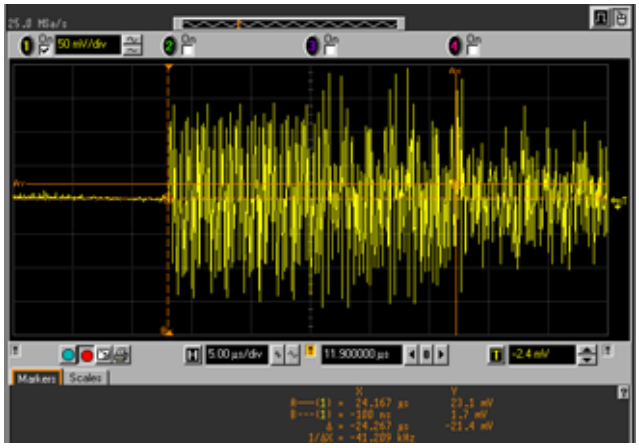


Figure 6. The preamble structure of IEEE802.16a

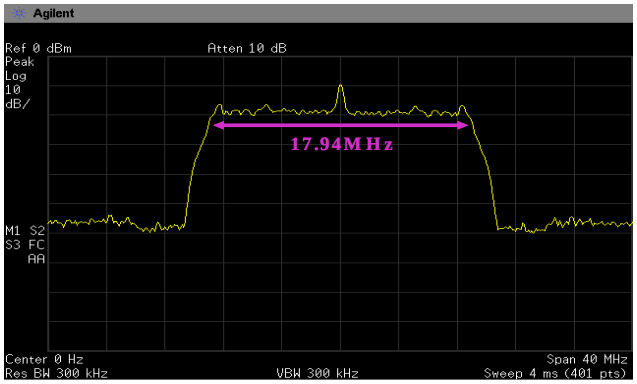
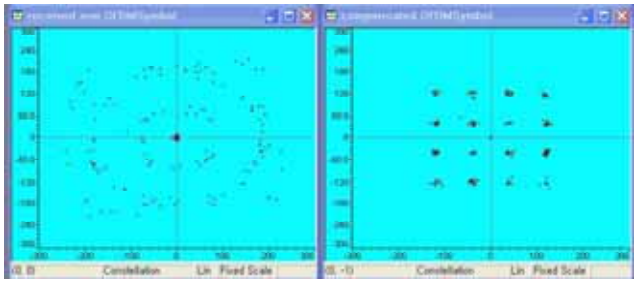


Figure 7. The signal spectrum of the IEEE802.16a

Figure 8-(a) shows the constellation of received signal with phase noise and Figure 8-(b) shows the channel compensated constellation.



(a) With phase noise (b) Channel compensated

Figure 8. The constellation of received signal

6. CONCLUSIONS

A SDR baseband platform for OFDM communication systems has been developed using three TI' TMS320C6416 fixed point DSP processor operating at the frequency of 720MHz and one Altera' EP1S40B968C6 Stratix FPGA. The DSP software for transmission was developed employing one DSP processor, and its achieved total cycle counts for one OFDM symbol (IEEE802.16a) generation is 4,695 cycles as shown in table 2. In receiver part, the DSP software developed using two DSP processors for real-time implementation. Synchronization algorithms (Frame and Symbol Detection, Channel Estimation) is done by DSP Rx1 processor and one received OFDM symbol (IEEE802.16a) is processed in 9,226 cycles by DSP Rx1 and Rx2 processors, as shown in table 2. Now, we are working on improvement of the developed SDR baseband platform and DSP software optimization for real-time implementation.

ACKNOWLEDGMENT

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7. REFERENCES

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