TEST RESULTS FOR A DIGITAL PREDISTORTION SYSTEM FOR 3G CELLULAR TELEPHONY

Gary Ragsdale (Southwest Research Institute, San Antonio, TX, gragsdale@swri.org)
Mike Pilcher (Southwest Research Institute, San Antonio, TX, mpilcher@swri.org.)
Travis Thompson (Southwest Research Institute, San Antonio, TX, tthompson@swri.org)

ABSTRACT

Southwest Research Institute® (SwRI®) has developed algorithms and a demonstration system for digital predistortion and is marketing contract engineering services to add digital predistortion capability to radio transmitters for customers not only in cellular telephony, but also in mobile video and even space. Digital predistortion (DPD) is an important enabling technology for software defined radio because it improves spectrum control and efficiency and can support more flexible radio frequency (RF) hardware. This paper describes our research results, focused on the 3G cellular market.

This research demonstrated the viability of these techniques through system simulations and hardware demonstration. In addition to software simulation, the researchers also performed hardware-in-the-loop (HIL) demonstrations, i.e., real hardware devices with personal computers (PCs) rather than digital signal processors (DSPs) for feedback signal processing. The HIL demonstrations validate the simulation and provide a realistic demonstration of crest factor reduction (CFR) and memory effects compensation (MEC) methods.

1. INTRODUCTION

Crest factor reduction (CFR) and memory effects compensation (MEC) are new digital predistortion (DPD) research topics in nonlinear device behavior, measurement, and compensation driven primarily by the recent adoption of multi-carrier broadcast standards. Basic research developed during the past four years promises new methods of implementing DPD within a cellular base station, high definition television (HDTV), and satellite transmitters. The research applies mathematical methods of predistorting the input signal to a nonlinear amplifier (Amp) to (1) cancel out large peaks in the amplifier input signal, which raise the "crest factor," and (2) compensate for the time-varying nonlinear amplifier transfer characteristic, commonly referred to as "memory effects."

CFR and MEC methods can significantly improve the power efficiency and lower the cost of constructing and operating high-power microwave amplifiers used in 3G cellular base stations, HDTV, military jamming, and automatic test systems. This research has already led to proposals for customer-funded research projects in the field of high-power microwave amplifier technology.

2. DIGITAL PREDISTORTION OVERVIEW

Microwave power amplifiers represent a significant portion of the cost and power consumption within microwave transmitters. There are an increasing number of applications that implement advanced system features and reduce system cost by combining multiple single-carrier transmitters into a single transmitter that broadcasts a multi-carrier signal [1].

Combining several carrier signals within the transmitter's power amplifier creates rapid variations in an amplifier's instantaneous output power, a condition described as high peak-to-average ratio (PAR) or as a high crest factor. If the amplifier is operating at a high average power output, with operation near its saturation region, and with a high peak to average power ratio (e.g., 9 to 15 decibels [dB]), then the amplifier will be randomly driven by the input signal peaks into a nonlinear operation region. If the amplifier gain and phase characteristics are time-invariant, then the amplifier exhibits a "memoryless" nonlinear behavior, i.e., it is a "memoryless amplifier."

Rapidly varying input power level will cause the amplifier integrated circuit die to rapidly heat and cool, and the amplifier direct current (DC) bias circuits may not adequately compensate for rapidly varying current drain under near saturation and high PAR operation. Thus, the amplifier may exhibit a time-varying nonlinear transfer characteristic referred to as memory effects behavior due to some combination of thermal hysteresis and DC bias modulation [2]–[6]. Combinations of high input signal PAR, memoryless nonlinear behavior, and memory effects behavior will produce FCC-prohibited adjacent channel and alternate channel interference unless steps are taken to compensate for amplifier design limitations.

Amplifier designers can mitigate the distortion caused by high PAR in several ways. The designer can increase the range of the amplifier linear operation region, improve the amplifier DC supply design, and/or use better transistor technology [4]. Problems with self-heating thermal hysteresis are especially difficult to eliminate. All of these design changes may reduce the nonlinear effects of a power amplifier. However, they can come at a much higher design and manufacturing cost.

It has been theorized and demonstrated by simulation (Sim) that methodical alteration (predistortion) of the multi-carrier input signal can improve the efficiency of high-power amplifiers [4][7]. Three methods have been theorized: crest factor reduction, memoryless DPD, and memory effects compensation. Crest factor reduction methods smooth the input signal peaks, thereby reducing the signal PAR and the probability of nonlinear excursions [8].

Memoryless DPD distorts the input signal in a way that compensates for a memoryless (time invariant), nonlinear gain and phase characteristics at high instantaneous power levels, thereby allowing the amplifier to operate at a higher power and PAR [9]. Prior work demonstrates that memoryless DPD significantly reduces adjacent channel and alternate channel interference within memoryless, multi-carrier transmitter systems.

Figure 1, a screen-shot from a Rhode and Schwarz (R&S) FSQ 26 Spectrum analyzer, illustrates the effects of power amplifier nonlinearities on a 20 MHz signal at 2.14 GHz and the potential spectral improvements offered by memoryless DPD. However, it will be shown that this memoryless DPD is ineffective when used with an amplifier that exhibits time variant, nonlinear gain characteristics (memory effects).

MEC methods distort the input signal to compensate for the time-varying gain and phase characteristics. MEC methods are the latest and most complex form of DPD. The methods hold great promise for improving performance and efficiency in high-power, wideband RF amplifiers.

Recent developments in high-speed integrated circuits make it possible to implement MEC and CFR methods within a combination of field programmable gate arrays and DSPs. Figure 2 illustrates the proposed DPD architecture of a microwave power amplifier using a predistorter field programmable gate array (FPGA) and a DSP control processor.

3. MEMORYLESS DPD

SwRI is developing DPD technology using a combination of detailed DPD software simulations and HIL demonstrations. The focus is on memoryless and memory amplifier performance when used with combinations of memoryless DPD, CFR, and MEC.

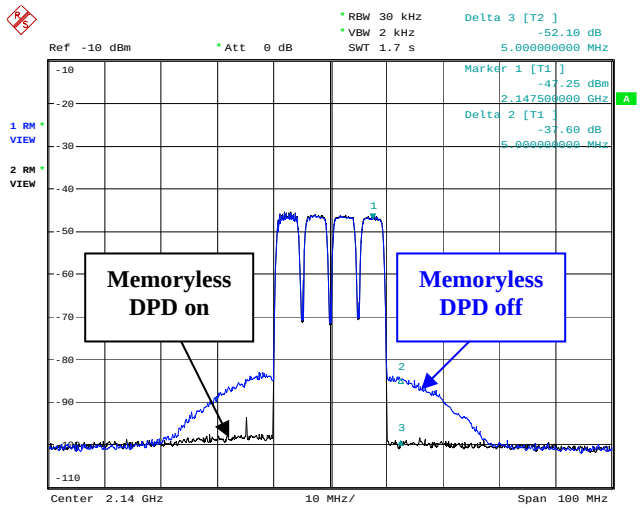


Figure 1. Nonlinearity Compensation Using Memoryless DPD

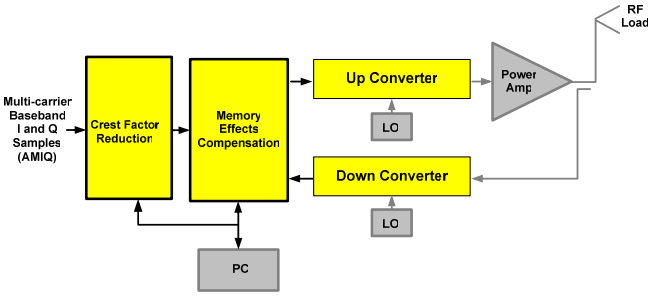


Figure 2. DPD Architecture for Memory Amplifiers

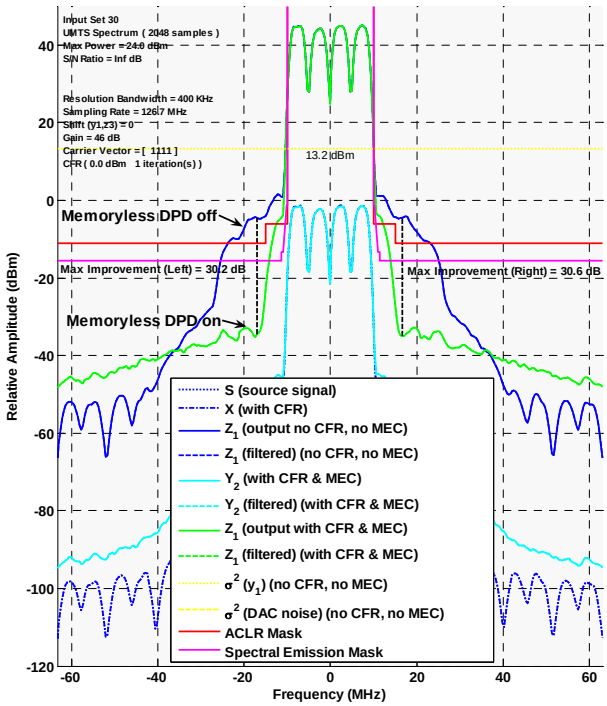


Figure 3. Memoryless Amp with Memoryless DPD Sim (no CFR)

3.1. Memoryless Amplifier Simulation

SwRI configured its DPD Simulation System to recreate a memoryless, 5th-order amplifier compensated by memoryless DPD amplifying a UMTS (Universal Mobile Telephone Service) test signal. The simulation did not apply crest factor reduction to the test signal. Figure 3 shows the results of the simulation. The solid blue trace (Z1) depicts the amplifier spectral output without DPD compensation. The uncompensated output exhibits an adjacent channel leakage ratio (ACLR) of approximately 45 dB. The solid green trace (Z1) depicts the amplifier output with memoryless DPD compensation. Figure 3 illustrates that an ACLR improvement of 30 dB is possible using memoryless DPD with a memoryless amplifier.

3.2. Memoryless Amplifier DPD Lab Results

SwRI applied memoryless DPD to a low-power, relatively memoryless Minicircuits amplifier using an Intersil ISL5239 Demonstration System. The Demonstration System stimulated the amplifier input with a UTMS test signal having an input power of -10 dBm. The amplifier average output power was 11 dBm. Figure 1 shows that the Minicircuits amplifier responded to memoryless DPD with an ACLR improvement of about 16 dB.

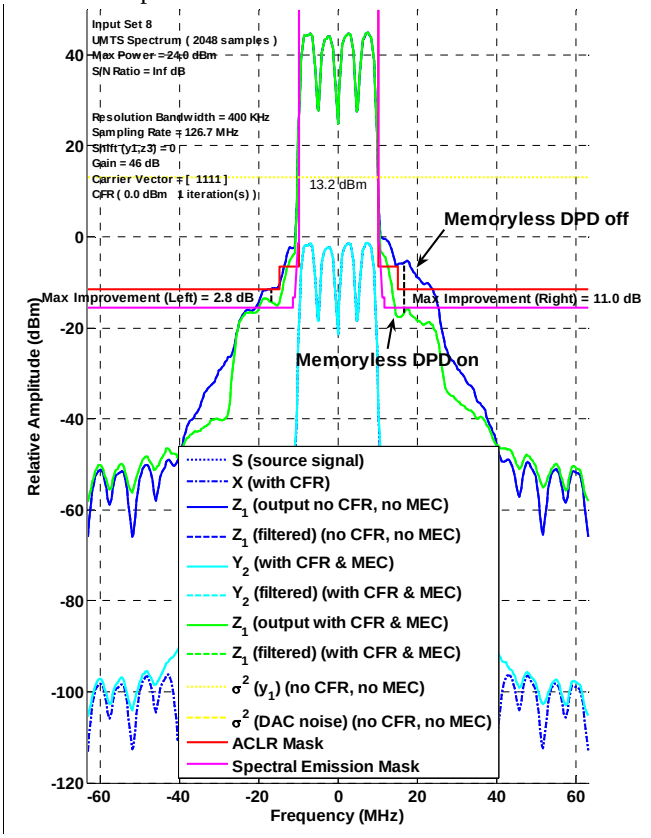


Figure 4. Memory Amp with Memoryless DPD Sim (no CFR)

3.3. Memory Amplifier with Memoryless DPD

As noted earlier, amplifier memory effects cannot be effectively compensated by a memoryless DPD System. The impact of amplifier memory effects on memoryless DPD will be illustrated in the following sections.

SwRI configured the DPD Simulation System to apply memoryless DPD to an amplifier exhibiting memory effects and 46 dB linear gain. The DPD Simulation System configuration was designed to mimic the behavior of an Empower amplifier. The asymmetric shape of the out-of-band spectral components is indicative of a memory amplifier and is displayed in Figure 4.

The predicted ACLR improvement using memoryless DPD for a memory amplifier (Figure 4) is much less than the improvement predicted for a memoryless amplifier (Figure 3). The memoryless DPD improved output ACLR by only 11 dB for the adjacent channels to the right of the in-band spectrum and had negligible effect on the left. This is in sharp contrast to the 30 dB improvement for the memoryless amplifier. Clearly, memory effects have a large impact upon memoryless DPD performance. The severity of the memory effects directly affects memoryless DPD performance.

3.4. Empower Amplifier with Memoryless DPD

SwRI installed the Empower amplifier in the Intersil ISL5239 Demonstration System as shown in Figure 5. Preliminary examination of the Empower amplifier indicated memory effects behavior within the amplifier.

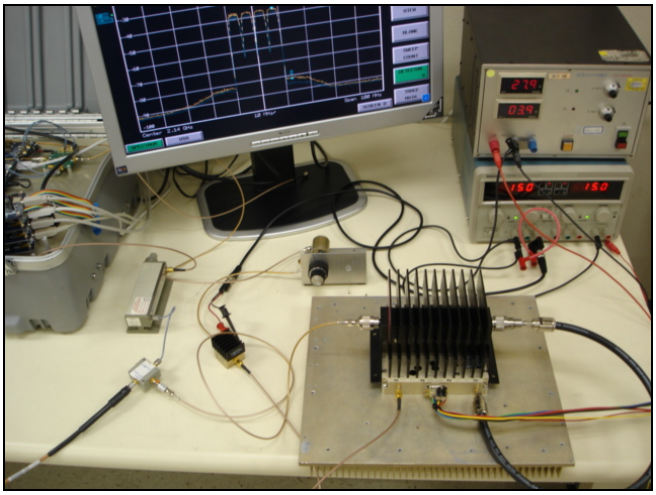


Figure 5. Empower Amplifier with Memoryless DPD

Figure 6 illustrates the results achieved by applying memoryless DPD to the Empower amplifier. The uncompensated amplifier output (shown as the black trace)

exhibited significant asymmetry. As in the simulation, one out-of-band shoulder was materially higher than the other out-of-band shoulder.

Memoryless DPD provided virtually no improvement in the Empower amplifier output ACLR. Figure 6 shows that memoryless DPD improved ACLR within the adjacent channels located to the left of the in-band spectrum (see the blue trace in Figure 6). There was a corresponding decrease in ACLR for the adjacent channels to the right of the in-band spectrum. The Empower amplifier memory effects appeared to be greater than the effects simulated in Figure 4. It is clear from the experiments that memory effects compensation is needed to improve the performance and efficiency of the Empower amplifier under test.

4. MEMORY AMP WITH MEC AND CFR DPD

It is also possible to apply combinations of MEC and CFR (CFR only, MEC only, or CFR plus MEC) to the amplifier as shown in Figure 2. The following sections will show that CFR improves ACLR in memory amplifiers. Appropriate application of MEC to a memory amplifier also improves ACLR in memory amplifiers. A combination of MEC and CFR achieves the highest possible ACLR improvement.

SwRI used the DPD Simulation System to predict ACLR performance for a system using CFR and MEC to linearize a memory amplifier. Figure 7 illustrates a typical simulation for a memory amplifier with CFR and MEC. The solid blue trace (Z1) depicts the amplifier spectral output without DPD compensation. The solid green trace (Z1) depicts the amplifier output with memoryless DPD compensation. The CFR-plus-MEC DPD improved output ACLR by more than 31 dB. Hardware experiments were conducted that verify CFR performance predictions. SwRI is developing an MEC system. It will be possible to measure MEC hardware performance in December 2005.

4.1. Comparison of DPD for Memory Amplifiers

SwRI performed a series of simulations using the SwRI DPD Simulation System to predict ACLR performance improvement achievable with CFR and MEC. The simulations specified a PAR reduction goal of 3.5 dB. The simulations specified an MEC design with compensation for 5th-order, time-variant distortion.

Table 1 summarizes the simulation results for an amplifier with no DPD compensation, with CFR compensation only, with MEC compensation only, and with CFR combined with MEC compensation. The simulations predict that significant improvement will be achieved using CFR or MEC. For example, the simulations predict that ACLR could be improved by 7 to 10 dB using CFR alone. There could be 27 to 29 dB of ACLR improvement using MEC alone. The greatest ACLR improvement occurs when CFR and MEC are used together with improvements in the range of 31 to 38 dB.

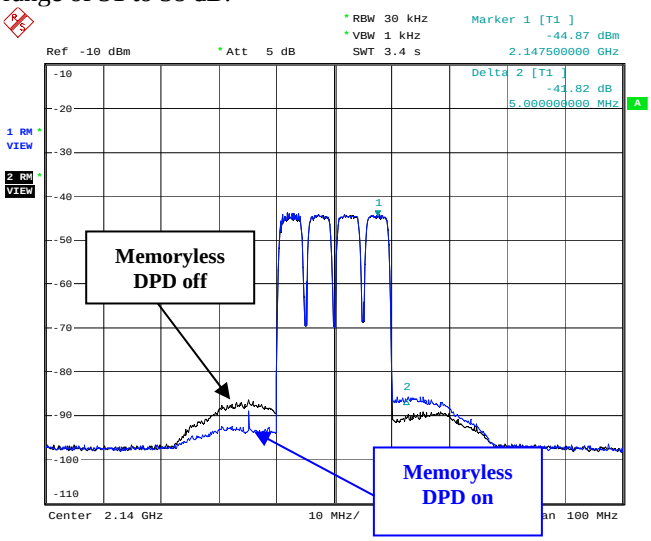


Figure 6. Memoryless DPD Applied to the Empower Amplifier

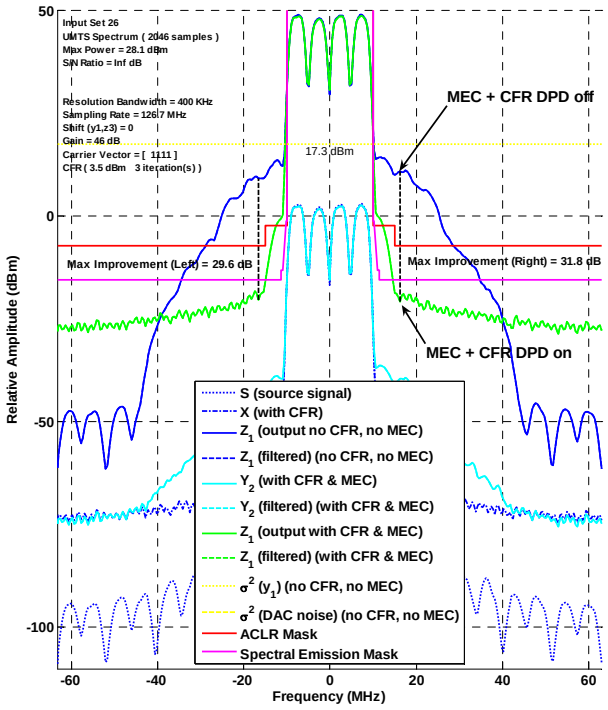


Figure 7. MEC and CFR with a Memory Amp

4.2. Crest Factor Reduction System Description

SwRI recently completed development of a CFR Demonstration System, shown in Figure 8. The System consists of an Altera FPGA evaluation board programmed with SwRI CFR firmware, an Intersil ISL5239 predistortion linearizer, and a Sorenza STQ-2016 direct RF up-converter.

Table 1 Amplifier ACLR for Alternative DPD Configurations

Uncompensated ACLR (dB marker-to-marker)	CFR-compensated ACLR (dB marker-to-marker)	MEC-compensated ACLR (dB marker-to-marker)	MEC Plus CFR ACLR (dB marker-to-marker)
30 dB	37 dB	57 dB	61 dB
35 dB	44 db	60 dB	76 dB
40 dB	50 dB	69 dB	78 dB

A Rohde and Schwarz AMIQ arbitrary signal generator provided a 10 MHz CDMA2000 test signal with eight modulated carriers as stimulus to the CFR FPGA evaluation board, and the PAR and ACLR reductions are measured on an R&S FSQ 26. Firmware resident in the FPGA performs all CFR-related signal processing.

The SwRI CFR method is a reconfigurable design implemented within an FPGA. It is possible to optimize the FPGA-based CFR design for resource consumption, latency, and error vector magnitude (EVM) within a set of design constraints.

The CFR algorithm is an iterative process of incrementally lowering the PAR of the signal through peak cancellation. The number of iterations is variable depending upon the available FPGA resources and the CFR system performance requirements. Laboratory experiments demonstrated a PAR reduction of over 3 dB for a 10 MHz CDMA2000 signal with eight active frequency allocations (FAs). The measurements were taken at a 10^{-4} complementary cumulative distribution function (CCDF) threshold as shown in Figure 9.

4.3. SEWON Teletech Amplifier with CFR FPGA

SwRI tested the CFR System with two high-power amplifiers. The first test was conducted using a SEWON Teletech LeanAmp STA2100-43MM-IB amplifier (SEWON amplifier) operating at a 46 dBm output power. The rated amplifier output power is 43 dBm. Figure 13 shows that CFR improved the SEWON amplifier output ACLR by approximately 15 dB.

4.4. EMPOWER Teletech Amp with CFR FPGA

SwRI used the CFR system to measure the effects of CFR compensation upon the Empower PCM5C5EAL amplifier (Empower amplifier). SwRI repeated the CFR experiment by first replacing the SEWON amplifier with the Empower amplifier. The CFR-compensated test signal level was adjusted to produce a 41 dBm output power. Figure 11 shows that SwRI's CFR system, using five iterations, improved the Empower amplifier output ACLR by approximately 11 dB.

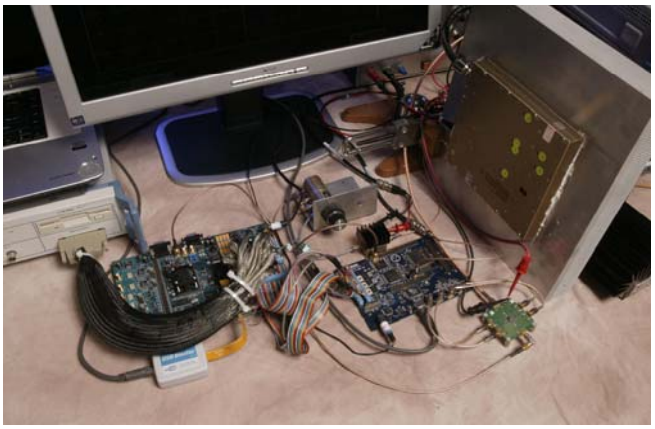


Figure 8. SwRI Crest Factor Reduction System

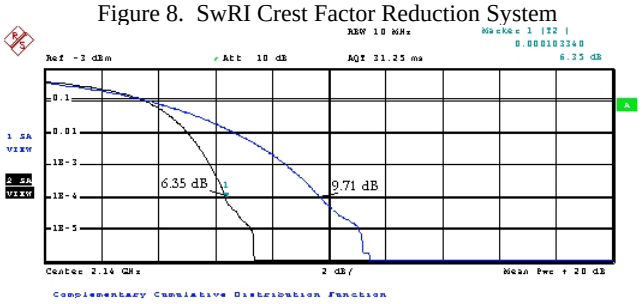


Figure 9. CCDF for 8-FA CDMA2000 Input Signal

5. CONCLUSIONS

SwRI used simulations and HIL tests to demonstrate the effectiveness of memoryless DPD, MEC, and CFR for multi-carrier, 3G cellular high-power RF amplifiers. Simulations and hardware experiments show that memoryless DPD works well only for memoryless amplifiers.

SwRI simulations predicted that the memory effects would render a memoryless DPD system ineffective. Experiments with high-power amplifiers, like the Empower and SEWON amplifiers, demonstrated the accuracy of the simulation predictions, both in spectral asymmetry and lack of material ACLR improvement. Improvement in memory amplifier performance requires some combination of CFR and MEC.

Crest factor reduction can produce significant ACLR improvement when used with memory (or memoryless) amplifiers. Experiments using the SwRI CFR system showed an 11 dB improvement in the Empower output ACLR. The SwRI CFR system improved the SEWON amplifier ACLR by 15 dB – even better than in simulation.

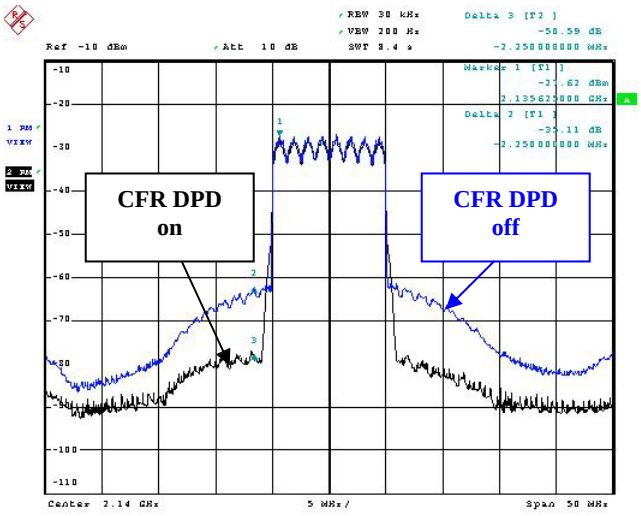


Figure 10. SEWON Amplifier (Actual Output Power = 46 dBm)

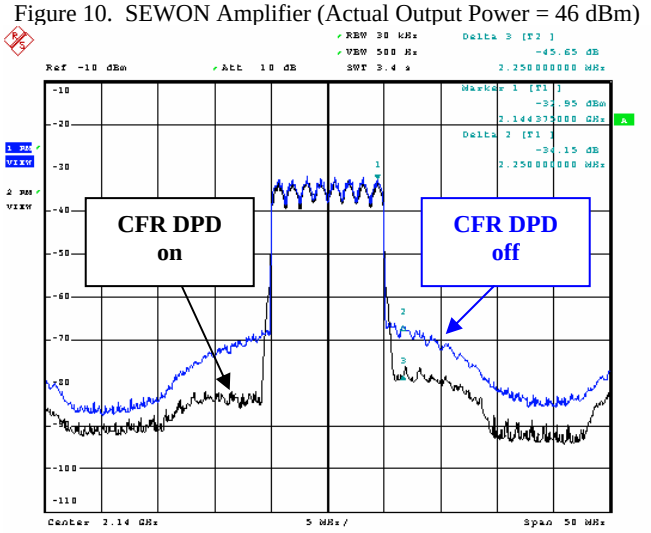


Figure 11. Empower Amplifier (Actual Output Power = 41 dBm)

CFR improves amplifier ACLR by reducing the PAR of the signal to be amplified. Reducing signal PAR reduces the impact of memoryless and memory effects distortion. However, CFR does not improve the linear behavior of the amplifier. Additional improvements in amplifier performance require compensation in the amplifier nonlinearity. CFR also makes the memoryless and MEC DPD algorithms more stable.

MEC counteracts the time-varying nonlinearity in memory amplifiers, thereby improving the amplifier output ACLR performance. Simulations show that MEC alone may improve memory amplifier ACLR by as much as 29 dB.

SwRI conducted simulations to examine the performance of CFR and MEC used in combination with a memory amplifier. The simulations show that the highest performance is achievable using both MEC and CFR DPD. ACLR improvement of up to 38 dB can be obtained by adding CFR to an MEC system. The ACLR improvement can be used to increase amplifier output power and efficiency.

Laboratory experiments with the SwRI CFR system show that the SEWON amplifier output power could be increased by about 3 dB with essentially the same ACLR. Simulations indicate that the combination of CFR and MEC might allow an increase in output power of up to 5 dB!

SwRI is currently developing DPD methods as a part of its software defined radio research and development program. SwRI recently completed development of a stand-alone flexible CFR device which is compatible with virtually any RF up-conversion design. SwRI will complete MEC FPGA firmware and associated DSP software during 2005.

6. REFERENCES

[1] "Operation and Performance of the ISL5239 Pre-Distortion Linearizer – AN1022," Intersil Corporation, July 2002.

[2] S.C. Cripps, *RF Power Amplifiers for Wireless Communications*, Artech House, 1999, ISBN 0-89006-989-1.

[3] W. Boesch and G. Gatti, "Measurement of Memory Effects in Predistortion Linearizers," 1989 IEEE MTT-S International Microwave Symposium Digest, Vol. III, June 13-15, 1989.

[4] S.C. Cripps, *Advanced Techniques in RF Power*, Artech House, 2002, ISBN 1-58053-282-9.

[5] J.F. Sevic, K.L. Burger, and M.B. Steer, "A Novel Envelope-Termination Load-Pull Method For ACPR Optimization of RF/Microwave Power Amplifiers," 1998 IEEE MTT-s IMS Digest, Vol. 2, pp. 723-726.

[6] S. David, W. Batty, A. Panks, R. Johnson, and C. Snowden, "Thermal Transients in Microwave Active Devices and Their Influence on Intermodulation Distortion," 2001 IEEE MTT-s IMS Digest, Vol. 1, p. 431-434.

[7] James B. Mullens, "Adaptive Predistortion Technique for Linearizing a Power Amplifier for Digital Data System," U.S. Patent 4,291,277, September 22, 1981.

[8] D.R. Gimlin and C.R. Patisaul, "On Minimizing the Peak-to-Average Power Ratio for the Sum of N Sinusoids," IEEE Transactions on Communications, Vol. 41, No. 4, April 1993.

[9] M. Faulkner and M. Johansson, "Adaptive Linearization Using Predistortion – Experimental Results," IEEE Transactions on Vehicular Technology, Vol. 43, No. 2, May 1994.

Test Results For A Digital Predistortion System For 3G Cellular Telephony

SDR'05 Technical Conference and Product Exposition
November 14 - 18, 2005

Presented by Gary Ragsdale, Ph.D.
Southwest Research Institute (SwRI)
GRagsdale@SwRI.org

Presentation Agenda

- Overview of digital predistortion
- Research goals and approach
- Comparison of digital predistortion techniques
- Comparison of simulations and HIL test results
- Future research in digital predistortion

Definition of Terms

- MCPA – multi-carrier RF power amplifier
  - Memoryless amplifier – input-invariant gain & phase characteristic
  - Memory amplifier – input-dependent gain & phase characteristic
- PAR – peak to average ratio
- ACLR – adjacent channel leakage ratio
- EVM – error vector magnitude
- DPD – digital predistortion
  - CFR – crest factor reduction
  - Memoryless DPD – memoryless digital predistortion
  - MEC – memory effects compensation
- FPGA – field programmable gate array
- GUI – software graphical user interface
- HIL – hardware-in-the-loop demonstration

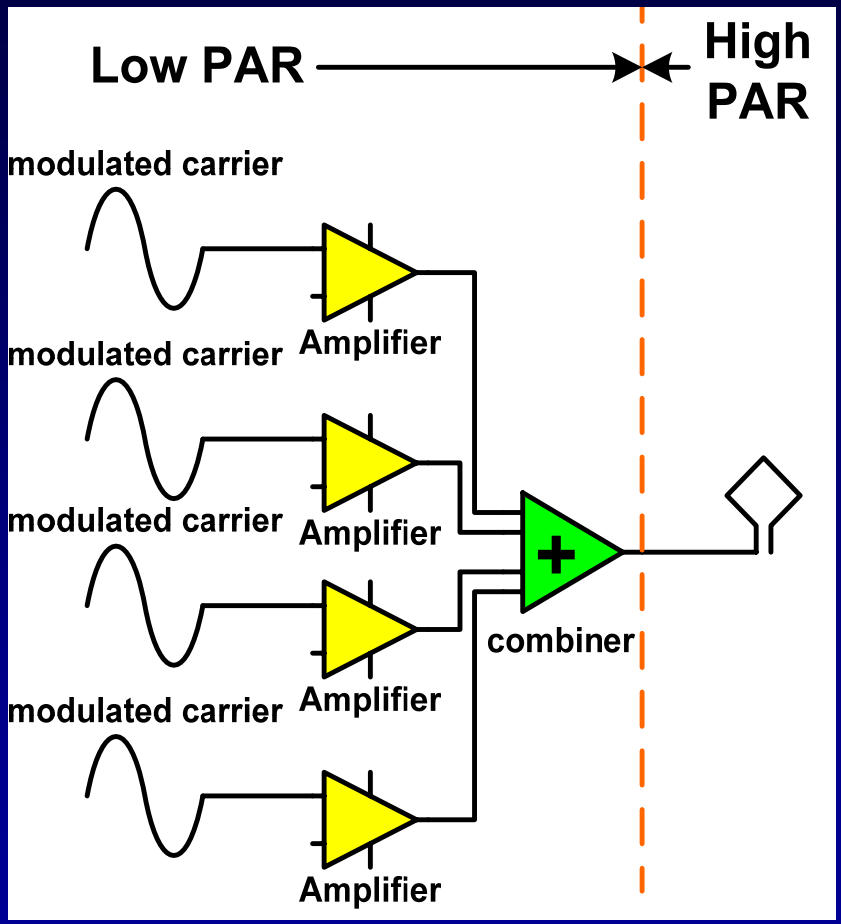
DPD Applications in RF Transmitters

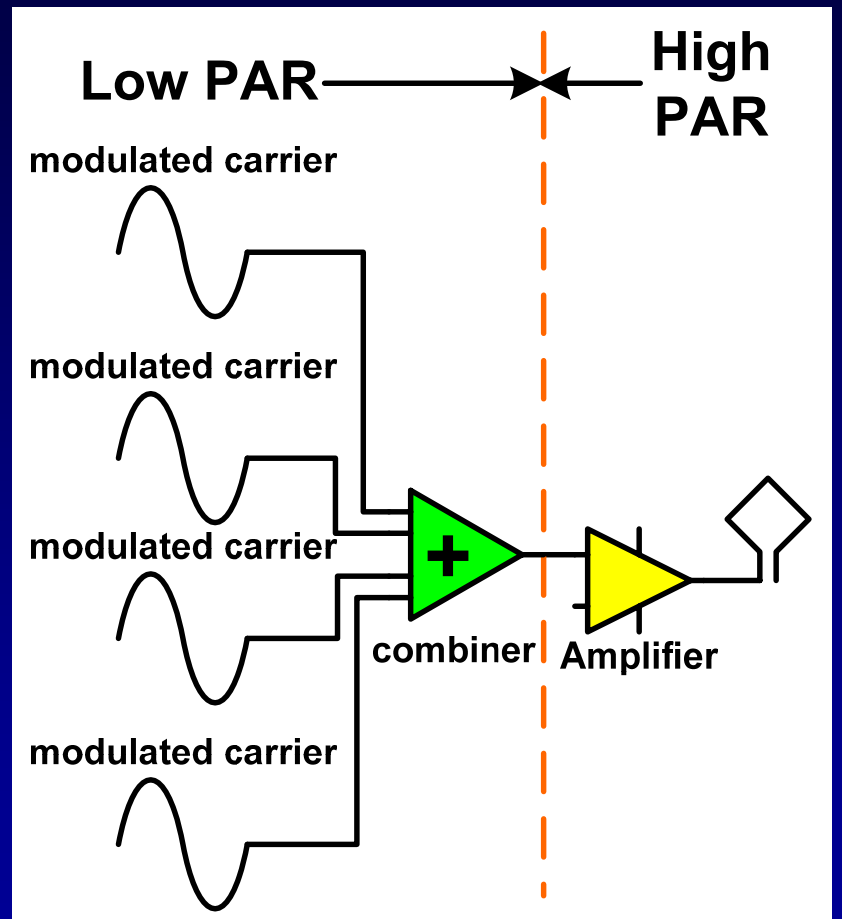
3G Cellular Telephone

Digital TV Broadcast

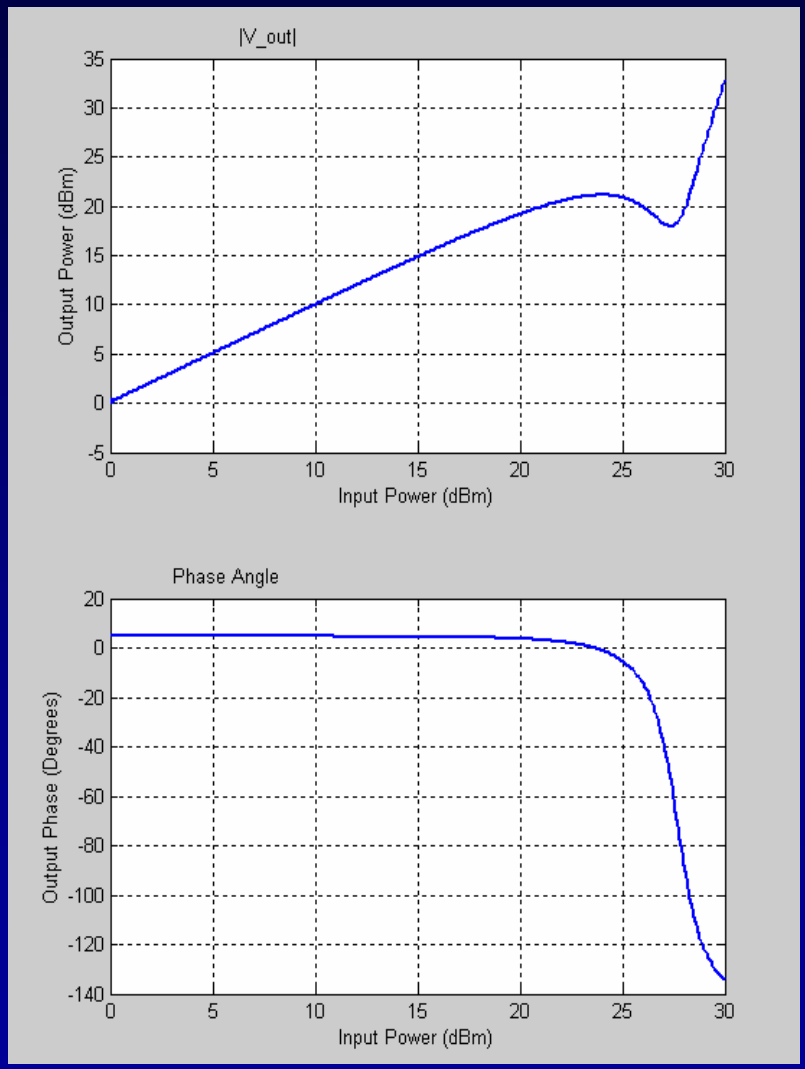
Satellite Stations & Orbiters

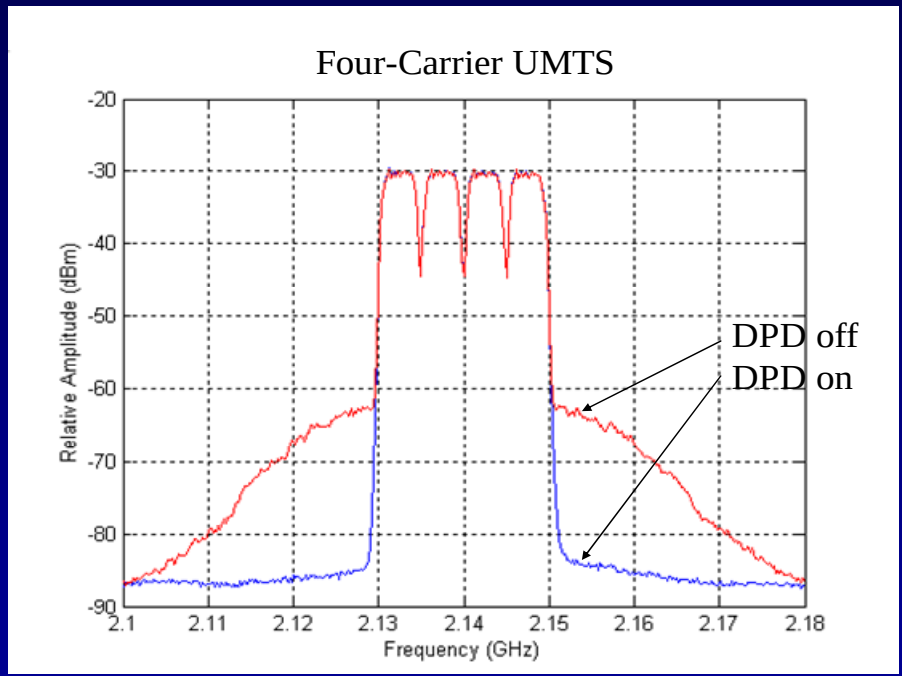
Creating High PAR within Multi-Carrier Signals



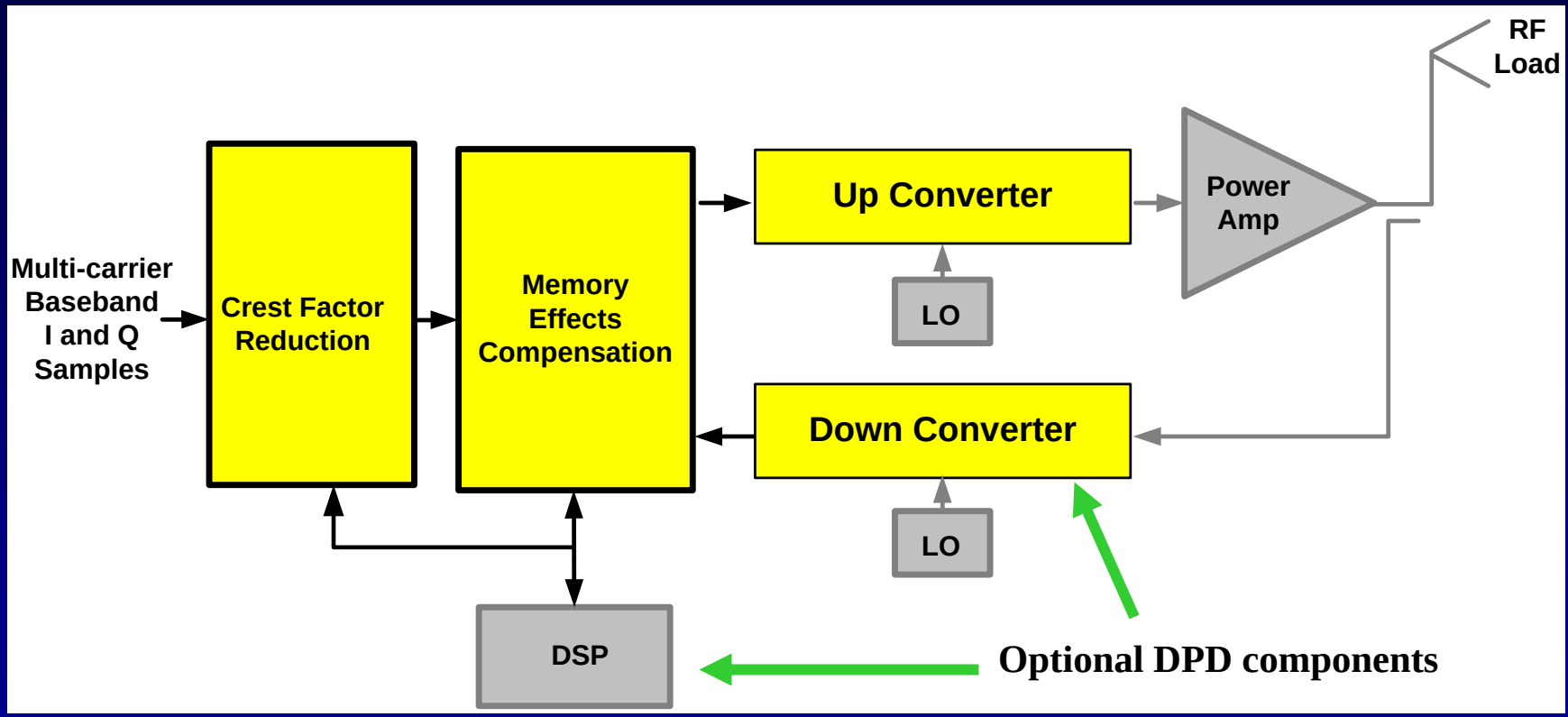


DPD Technology Overview

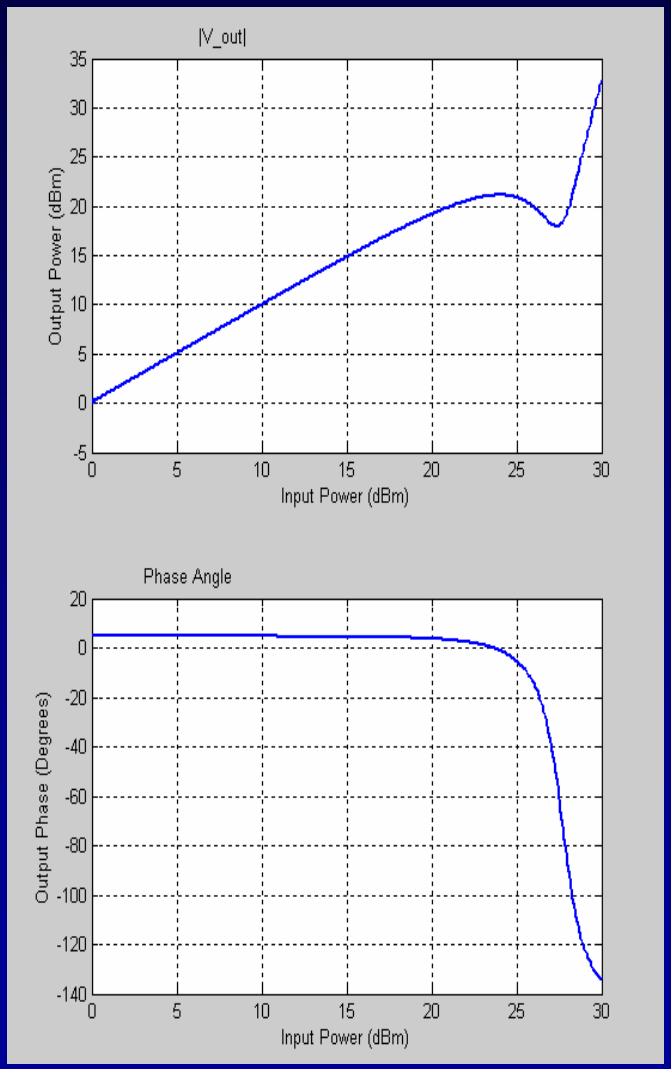


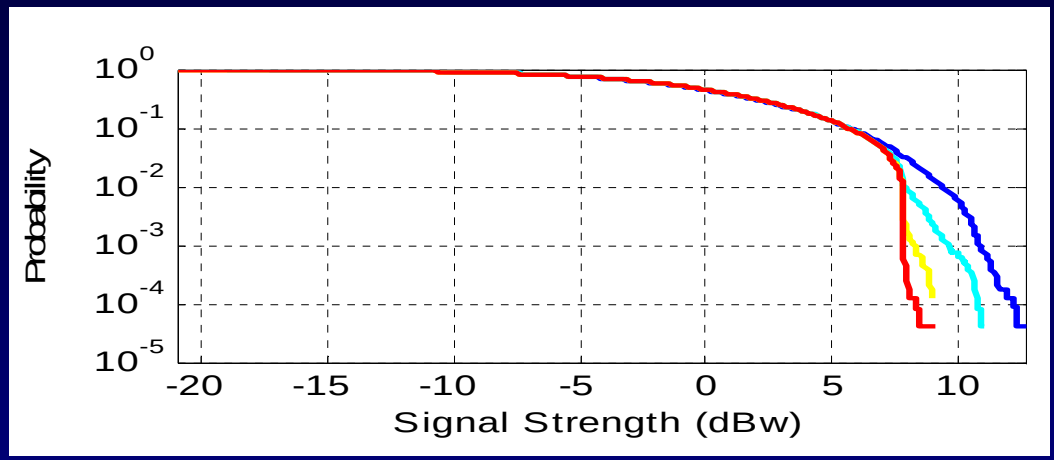


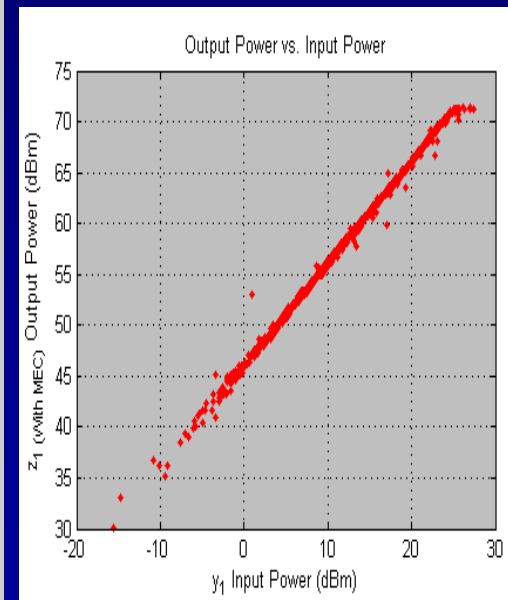
Digital Predistortion System Architecture

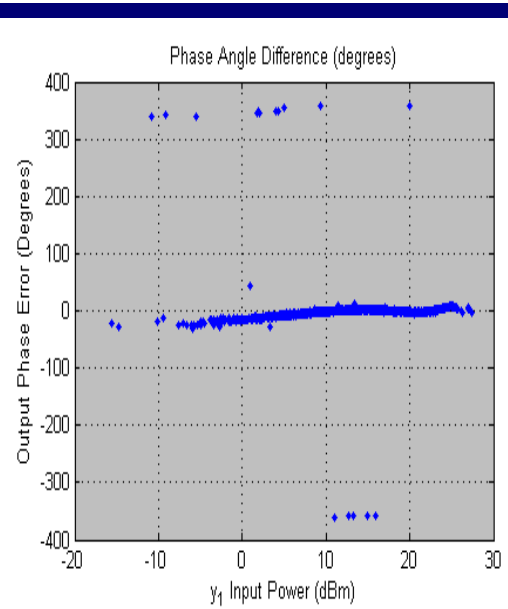


Linearizing MCPAs with Digital Predistortion

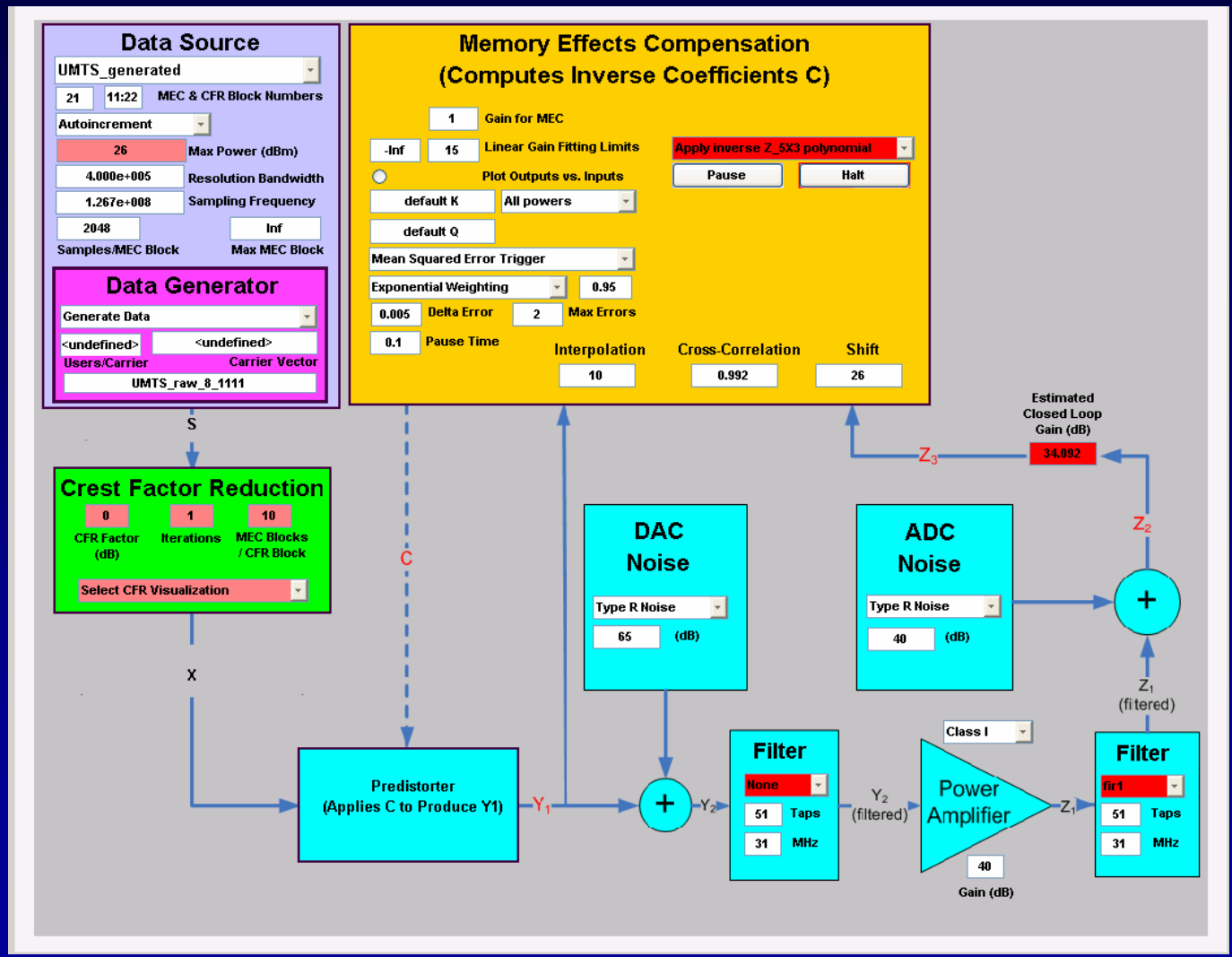




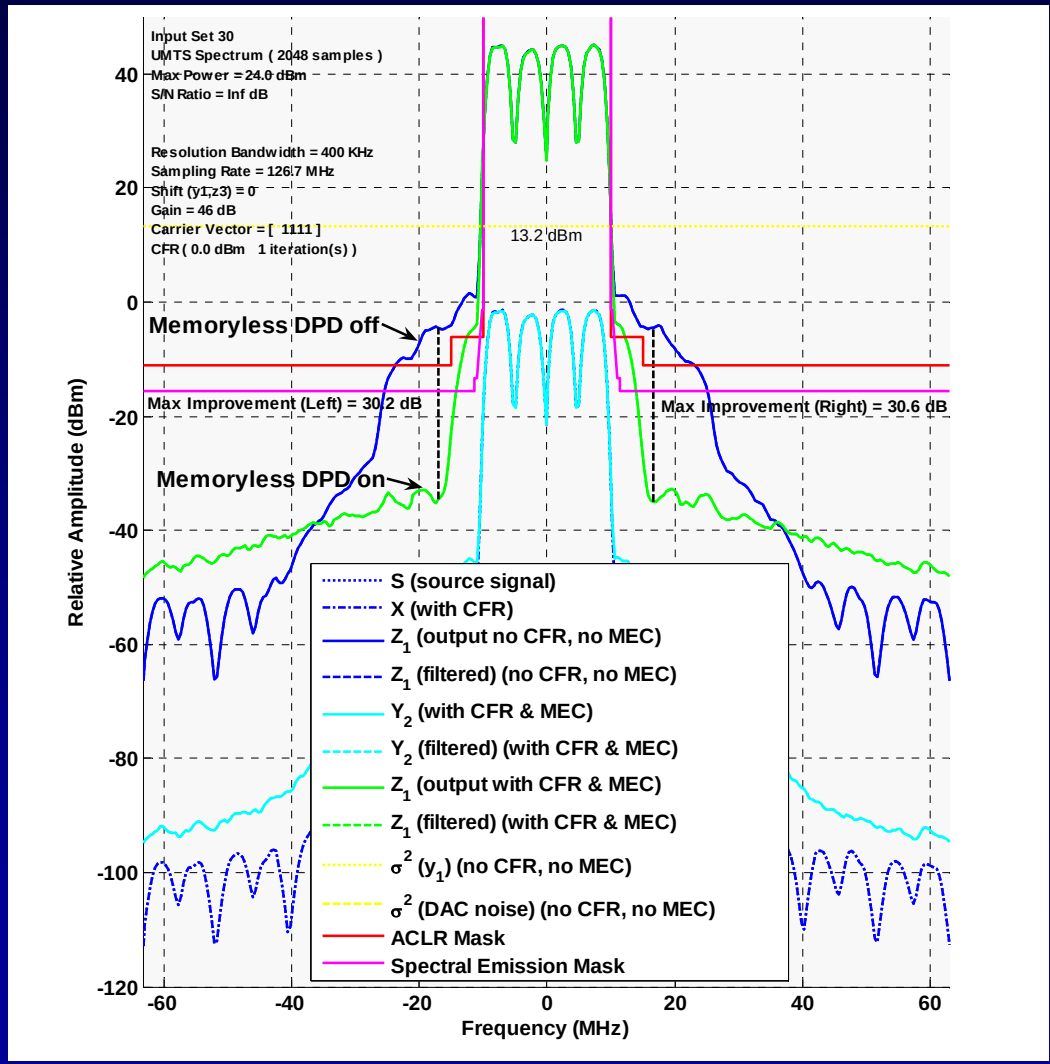




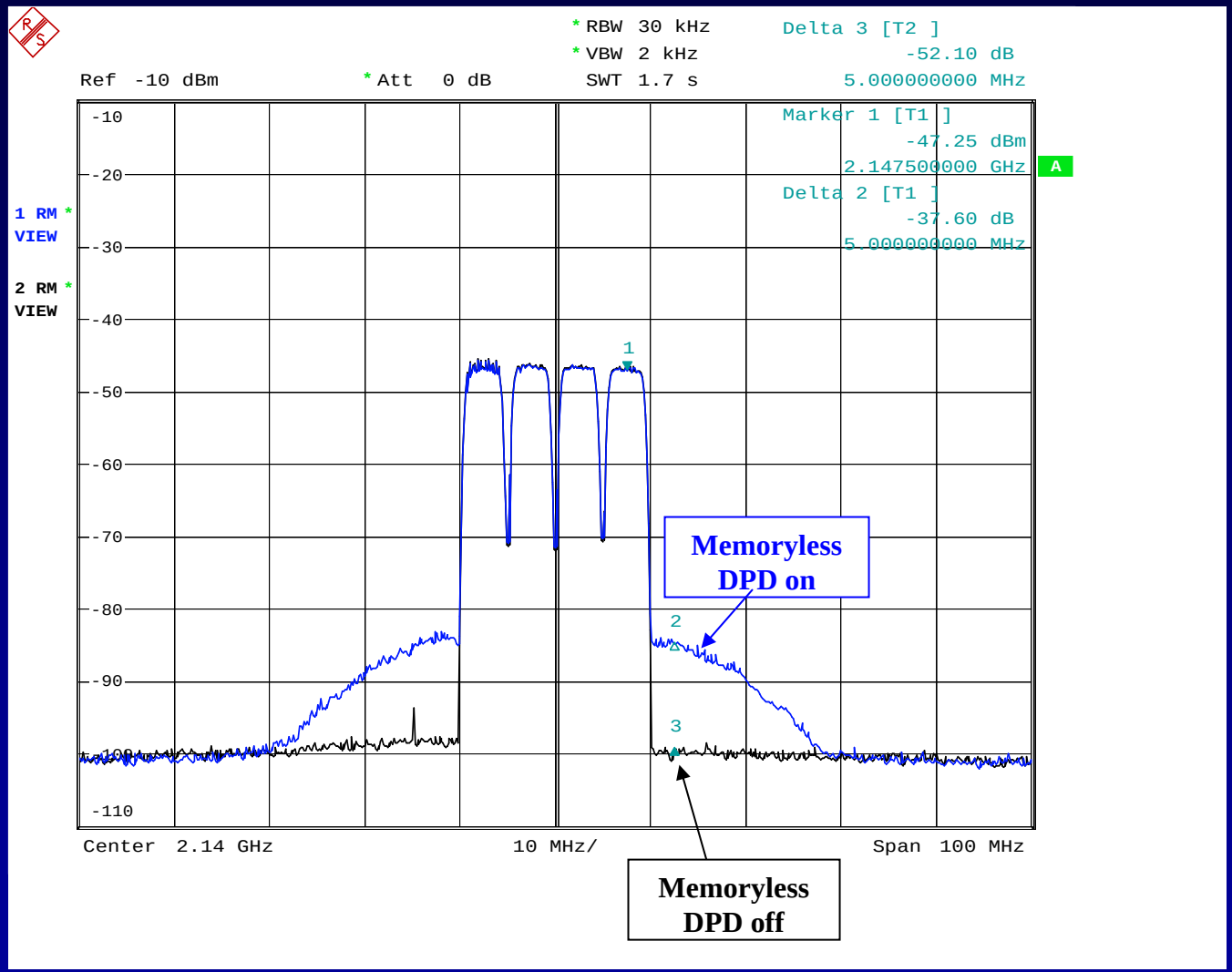
DPD Simulation and HIL System GUI



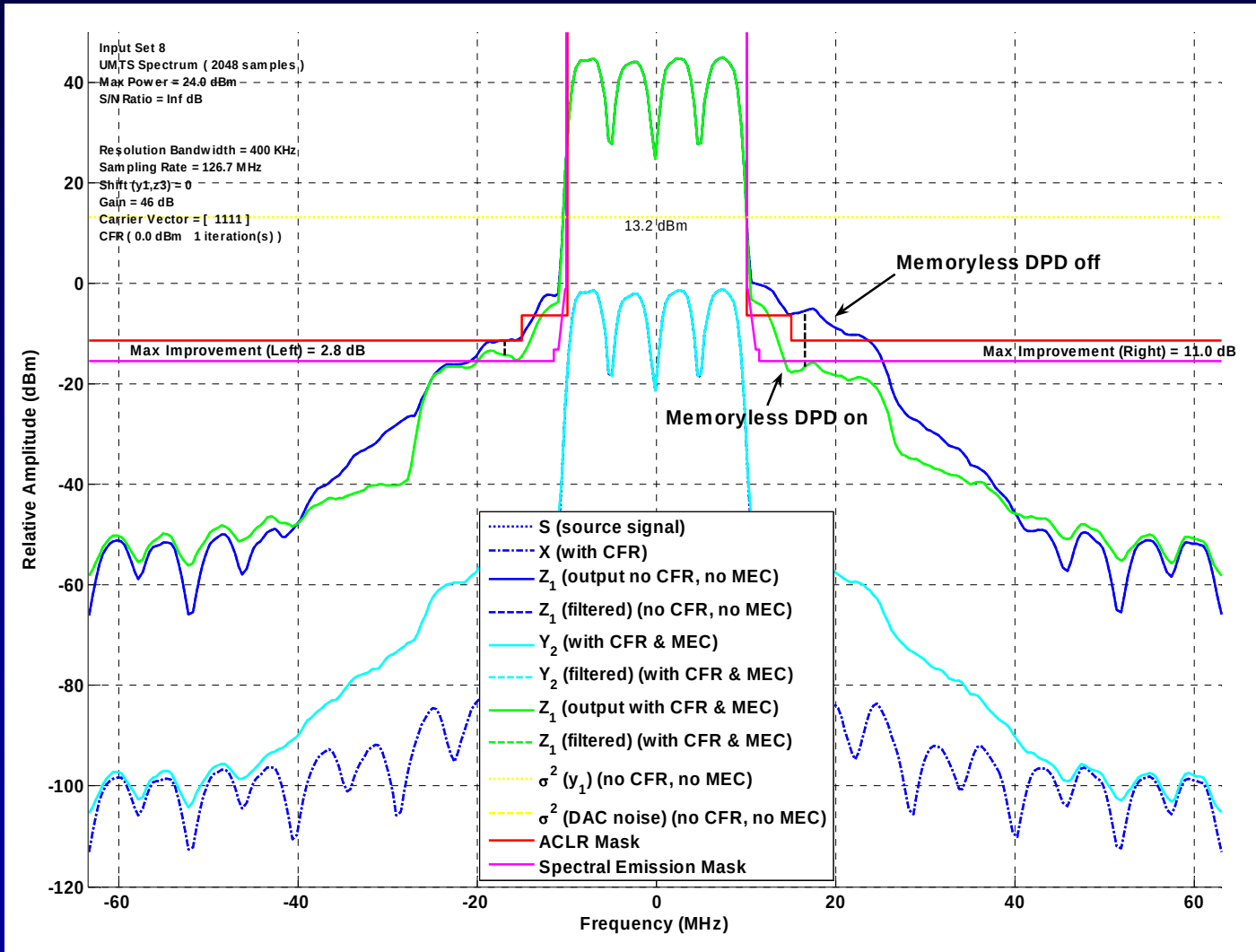
Memoryless DPD for Memoryless Amplifier SIM



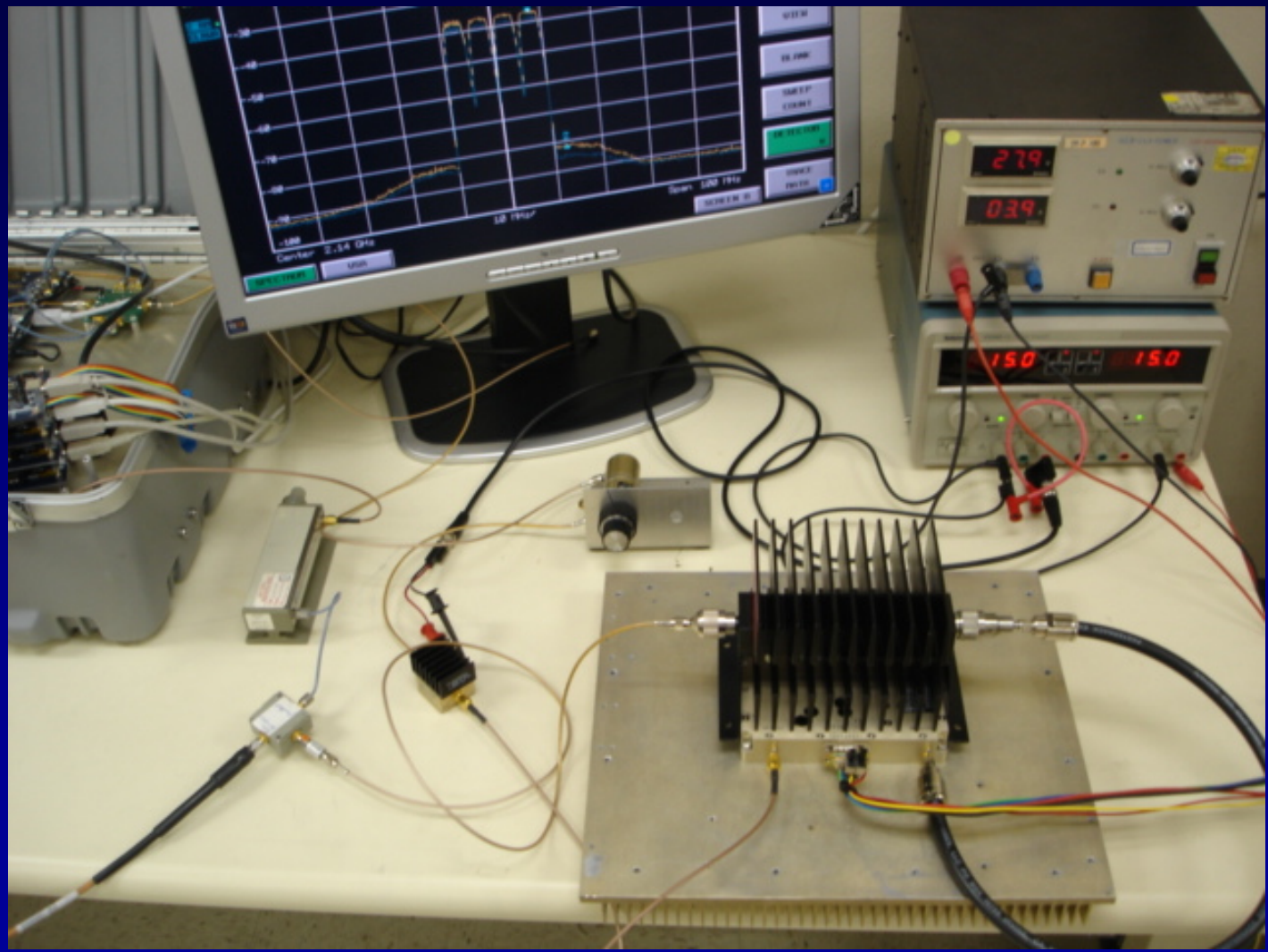
Memoryless DPD for Memoryless MCPA Measurement



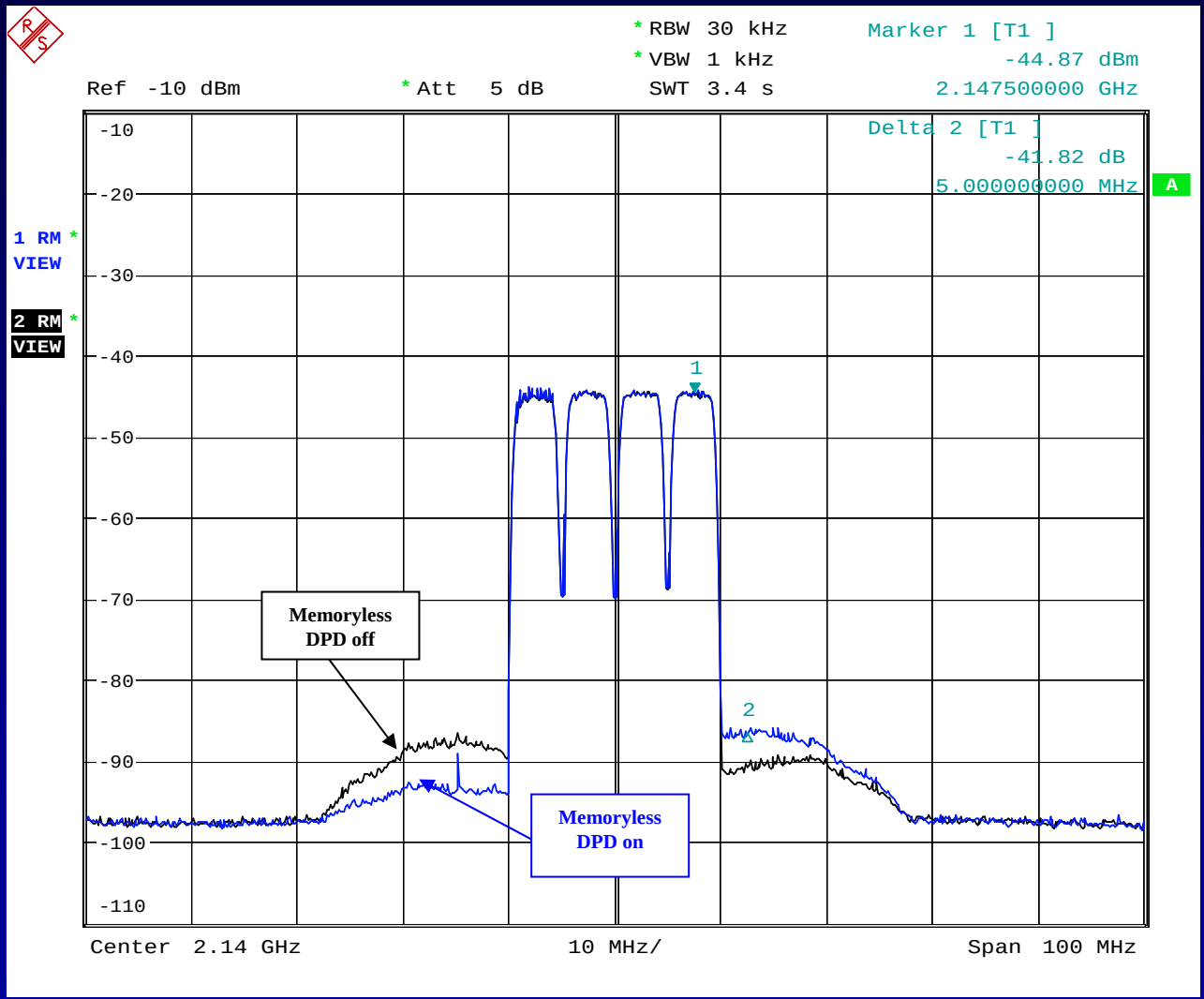
Memory MCPA with Memoryless DPD Sim (no CFR)



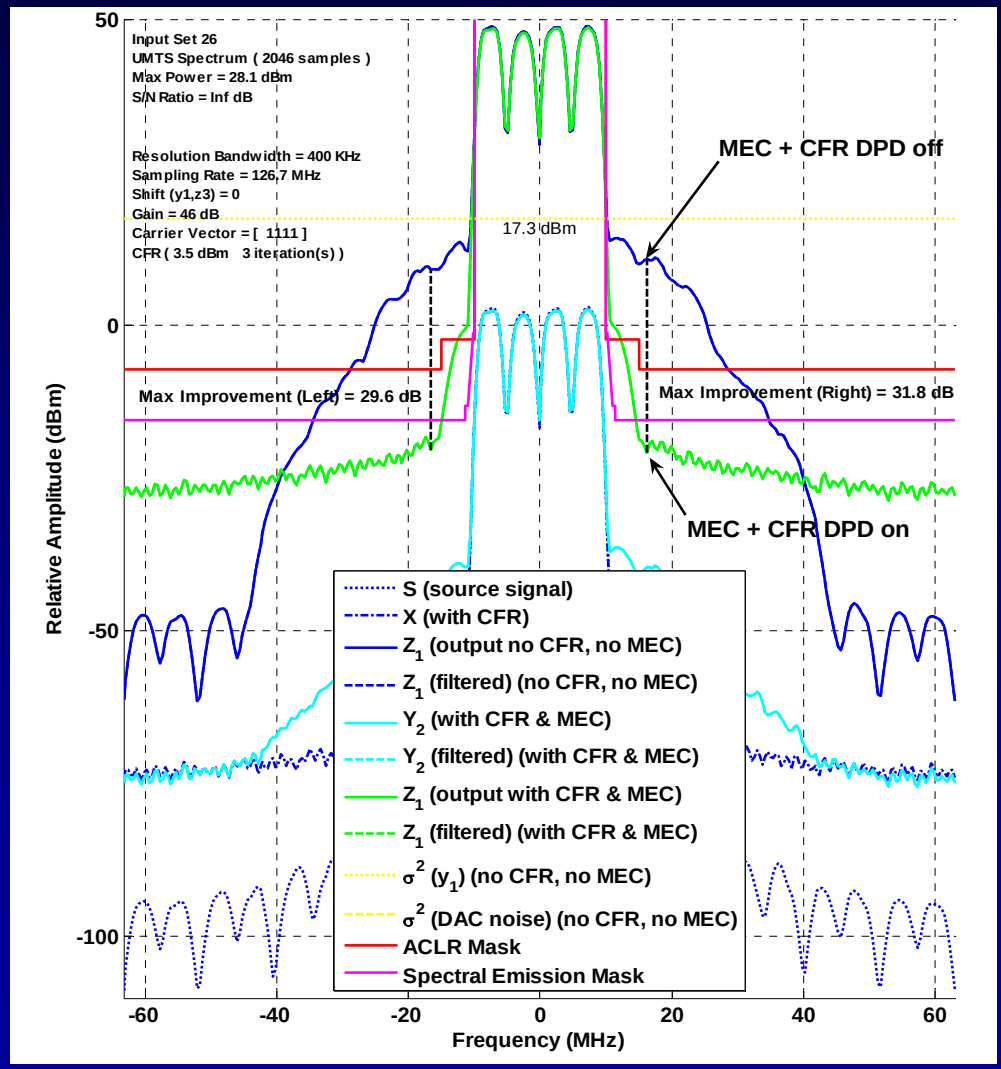
Empower MCPA with Memoryless DPD



Memoryless DPD Applied to Empower MCPA



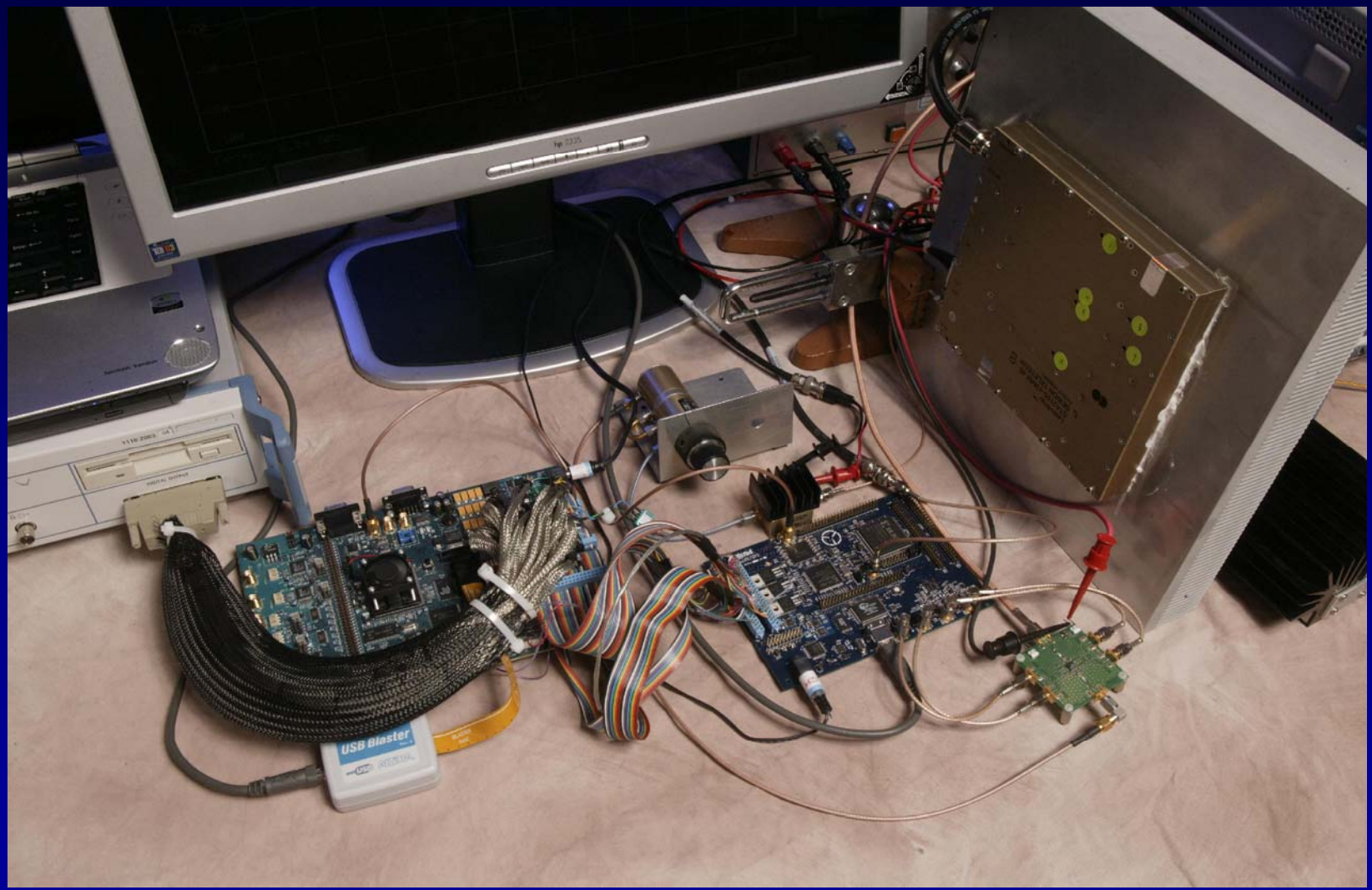
MEC and CFR with a Memory Amplifier



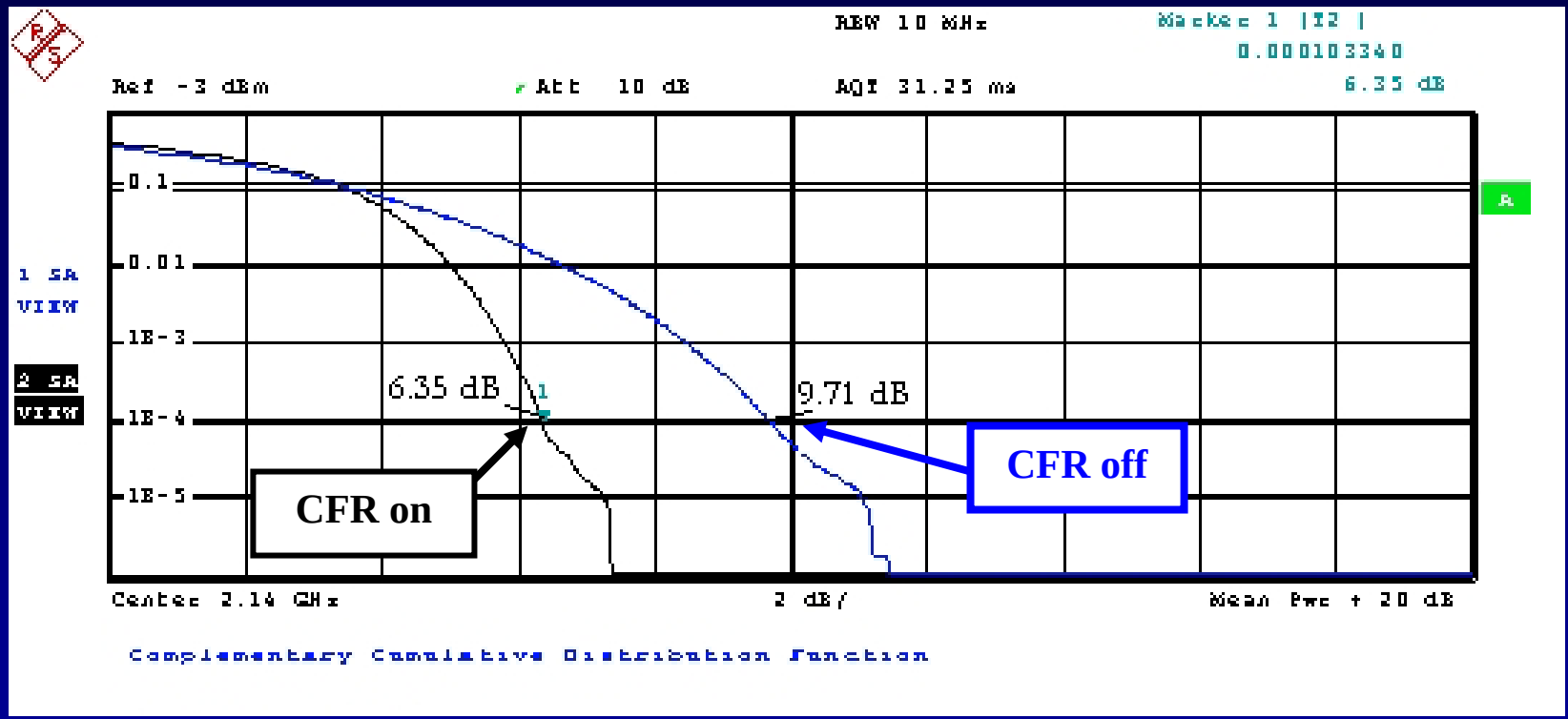
Amplifier ACLR for Alternative DPD Designs

Uncompensated ACLR (dB marker-to-marker)	CFR-compensated ACLR (dB marker-to-marker)	MEC-compensated ACLR (dB marker-to-marker)	MEC Plus CFR ACLR (dB marker-to-marker)
30 dB	37 dB	57 dB	61 dB
35 dB	44 db	60 dB	76 dB
40 dB	50 dB	69 dB	78 dB

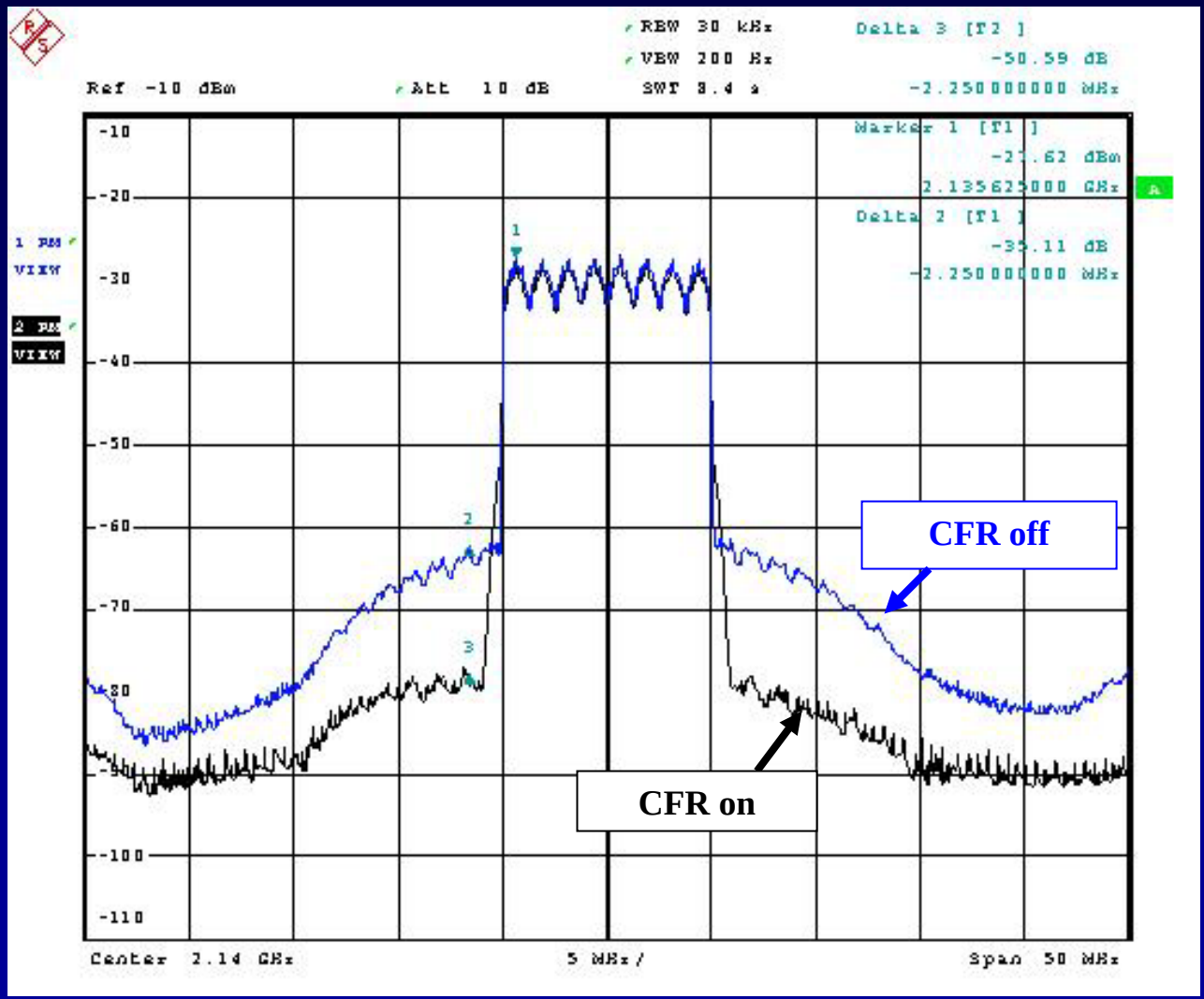
SwRI CFR System with SEWON MCPA



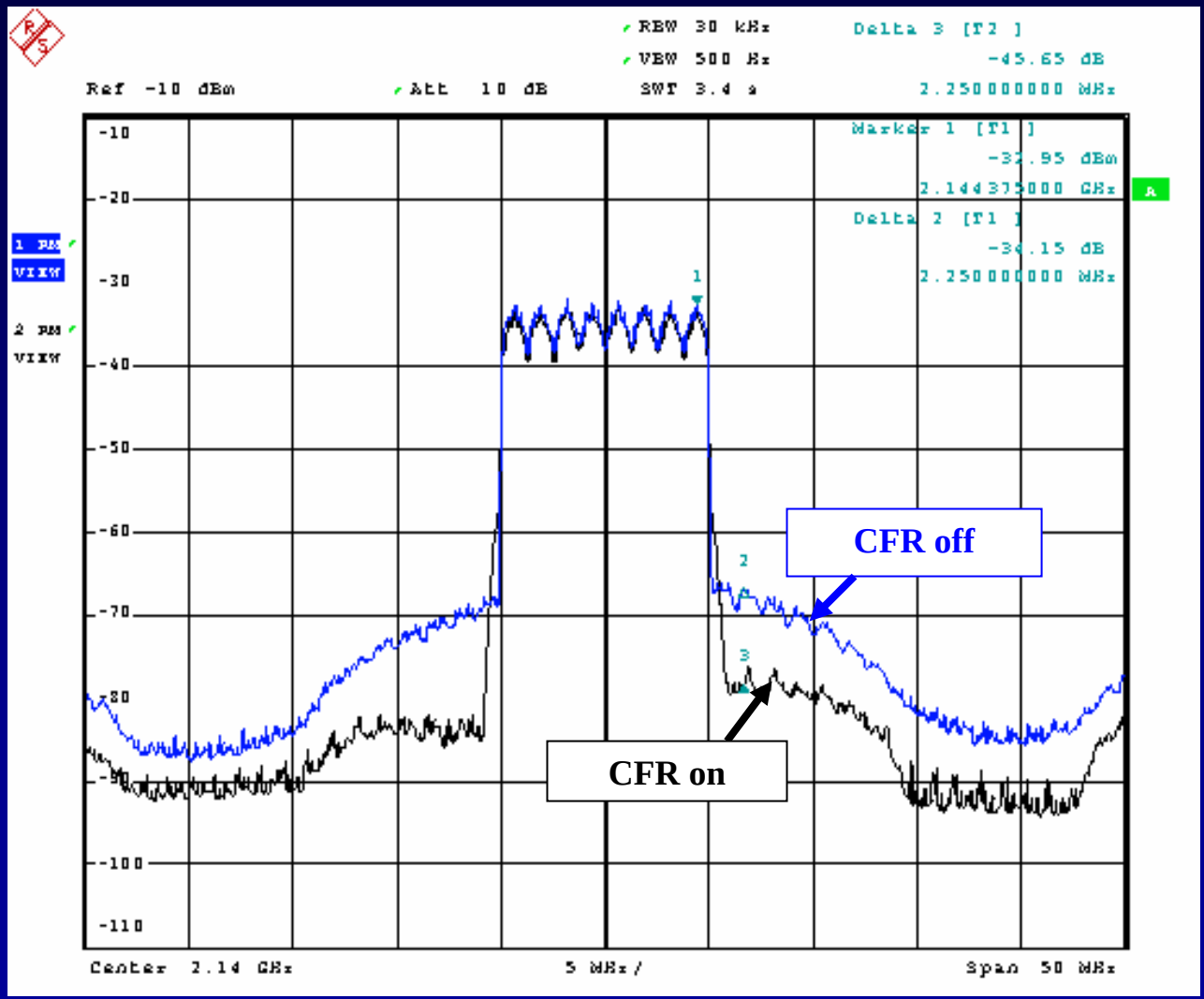
CCDF for 8-Carrier CDMA2000 Input Signal



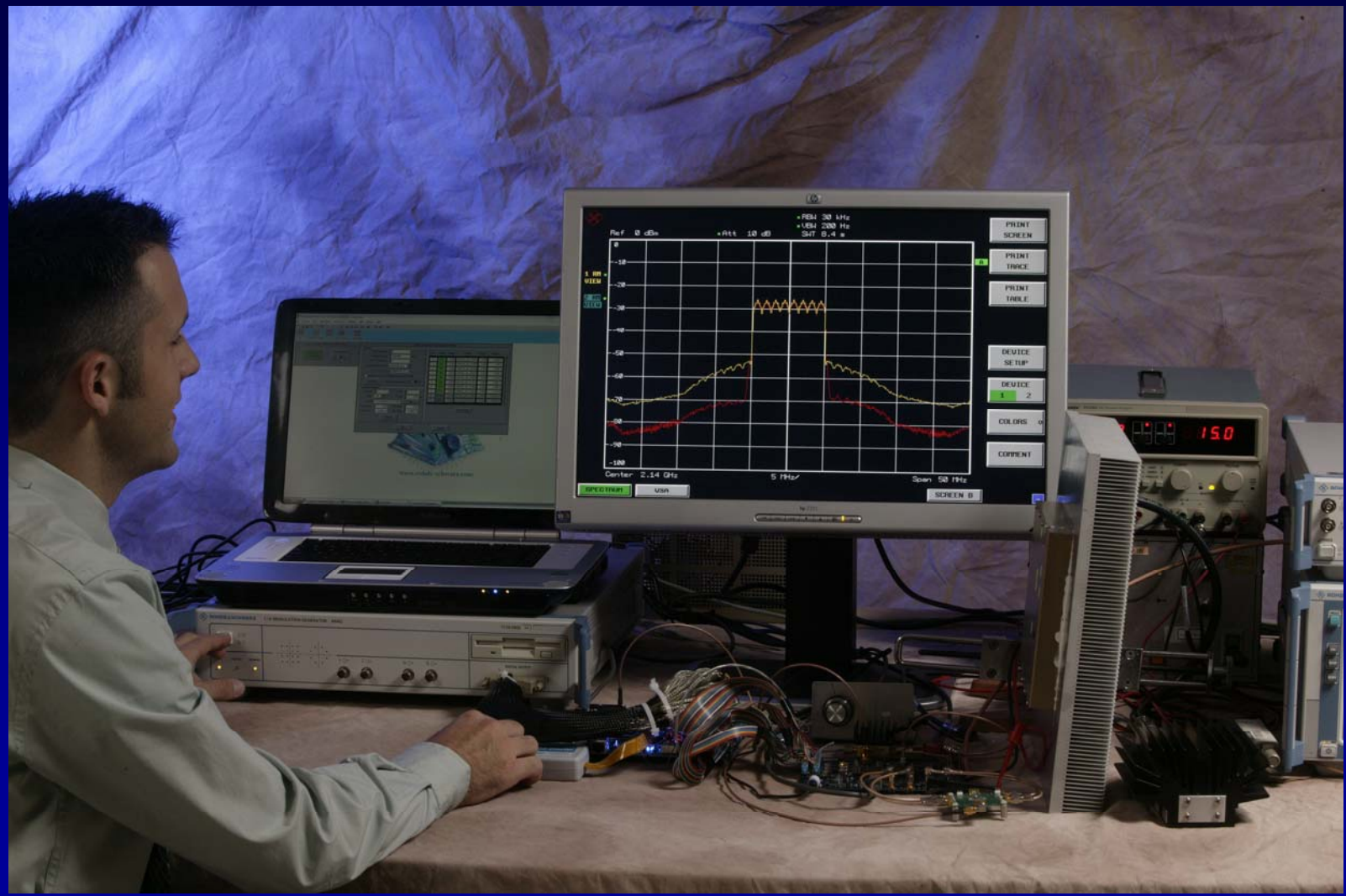
SEWON MCPA with CFR (Output Power = 46 dBm)



Empower MCPA with CFR (Output Power = 41 dBm)



Developing MEC for RF Systems in 2005



Considerations for DPD Future Research

- Modeling of high power MCPAs
  - Derive models directly from working amplifiers
  - Determine long-term drift in amplifier behavior
- Equalization of RF conversion components

Conclusions

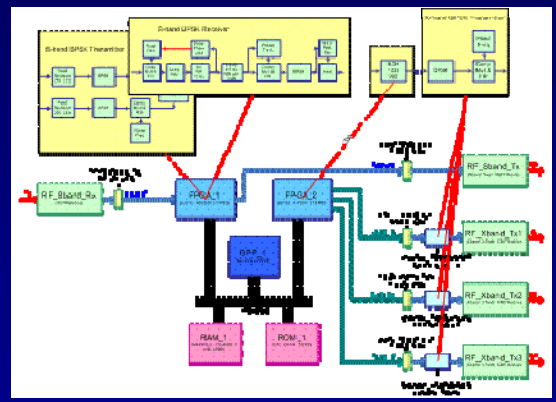
- Simulations predict substantial ACLR improvements
- HIL demonstrations support predictions
  - Results vary by amplifier design
  - Results vary by modulation method
  - Results affected by up and down conversion design
- Memoryless DPD works well for memoryless MCPAs
- SwRI CFR IP core improves MCPA performance
  - Reduces PAR 3.4 dB
  - Increases ACLR 10+ dB
- MEC FPGA & DSP operational by December 2005

SwRI Software Defined Radio Research Program

SDR Testbeds, Waveforms, and Architectures

Smart Antenna

Digital Predistortion



Design Tools