MIMO OFDM Transceiver for a Many-Core Computing Fabric – A Nucleus based Implementation

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Introduction

- **Nucleus Methodology**
- **MIMO OFDM Transceiver Implementation**
  - Application Analysis - Nuclei Identification
  - Efficient Nuclei Implementations on HW Platform (Flavor)
  - Algorithmic Performance Evaluation
  - Application-to-Architecture Mapping
- **Summary & Outlook**

Software Defined Radio Vision

Source:
Infineon Technologies

Source:
Infineon Technologies

Today's Mobile Phone

Future SDR Mobile Phone

The three key properties:

- **Portability**
  - Software is portable onto different platforms
    Standard.exe → *Device_1, ..., Device_n*

- **Interoperability**
  - Different devices configured for the same standard interoperate
    Standard_1/Device_1 ↔ *Standard_1/Device_2*

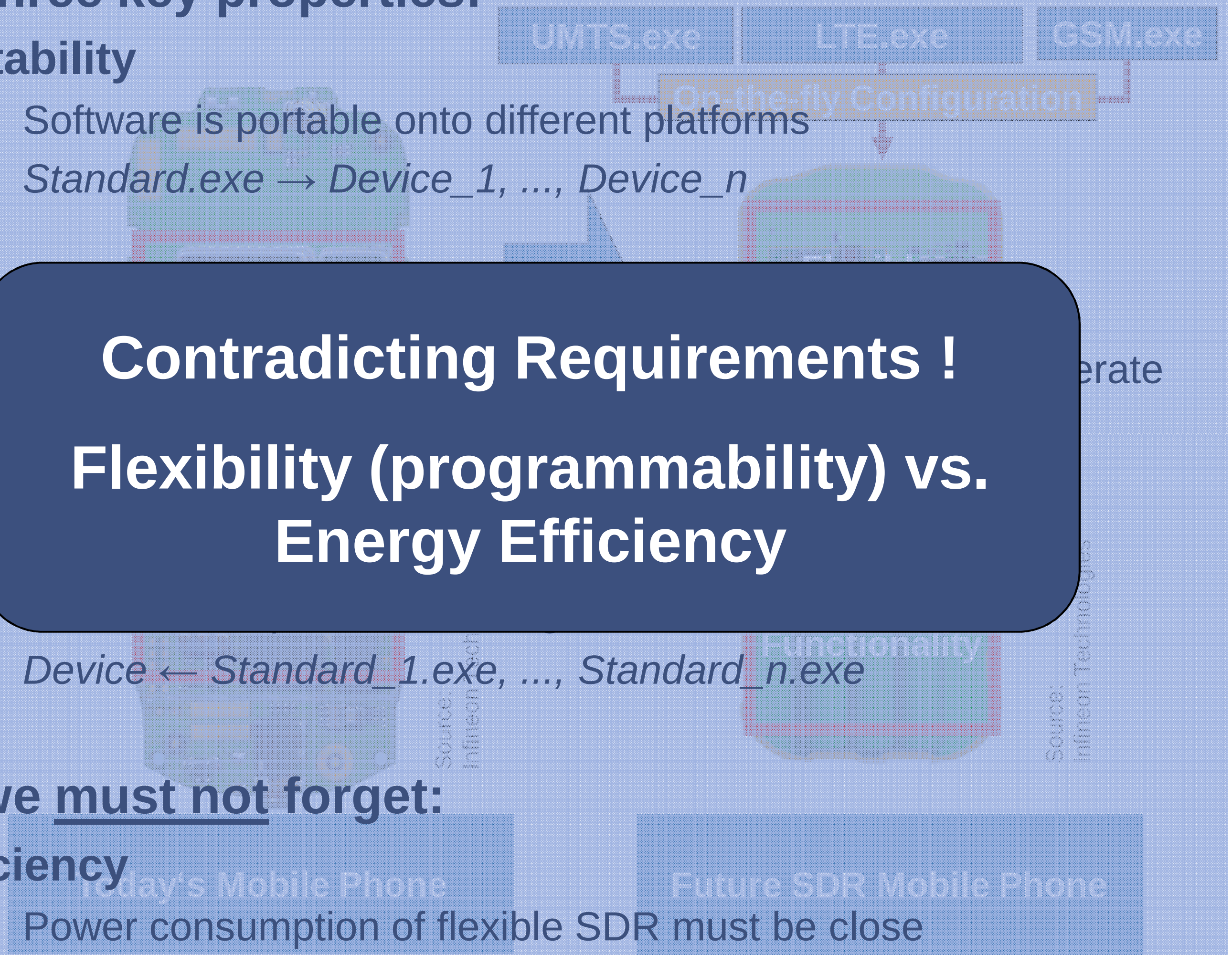
- **Loadability**
  - Platform is capable of running different standards
    Device ← *Standard_1.exe, ..., Standard_n.exe*

But we must not forget:

- **Efficiency**
  - Power consumption of flexible SDR must be close
    to power consumption of dedicated device (*battery driven!*)

The three key properties:

- **Portability**
  - Software is portable onto different platforms
    Standard.exe → Device_1, ..., Device_n
- **Inte**
  - erate
- **Loa**
  - *Device ← Standard_1.exe, ..., Standard_n.exe*



Contradicting Requirements !

Flexibility (programmability) vs. Energy Efficiency

But we <u>must not</u> forget:

- **Efficiency**
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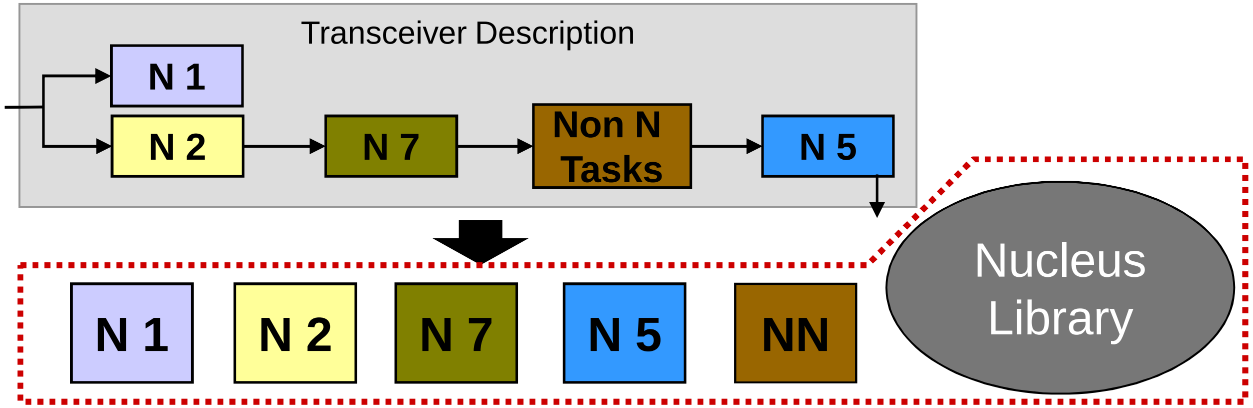
Nucleus Methodology

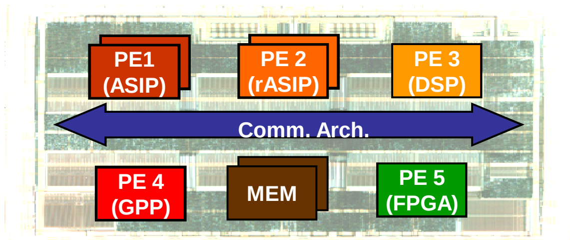
Transceiver Description



Nuclei

Nucleus
- Critical, demanding, algorithmic kernel
- Kernel is common among different waveforms
- Not waveform nor hardware specific

HW Platform



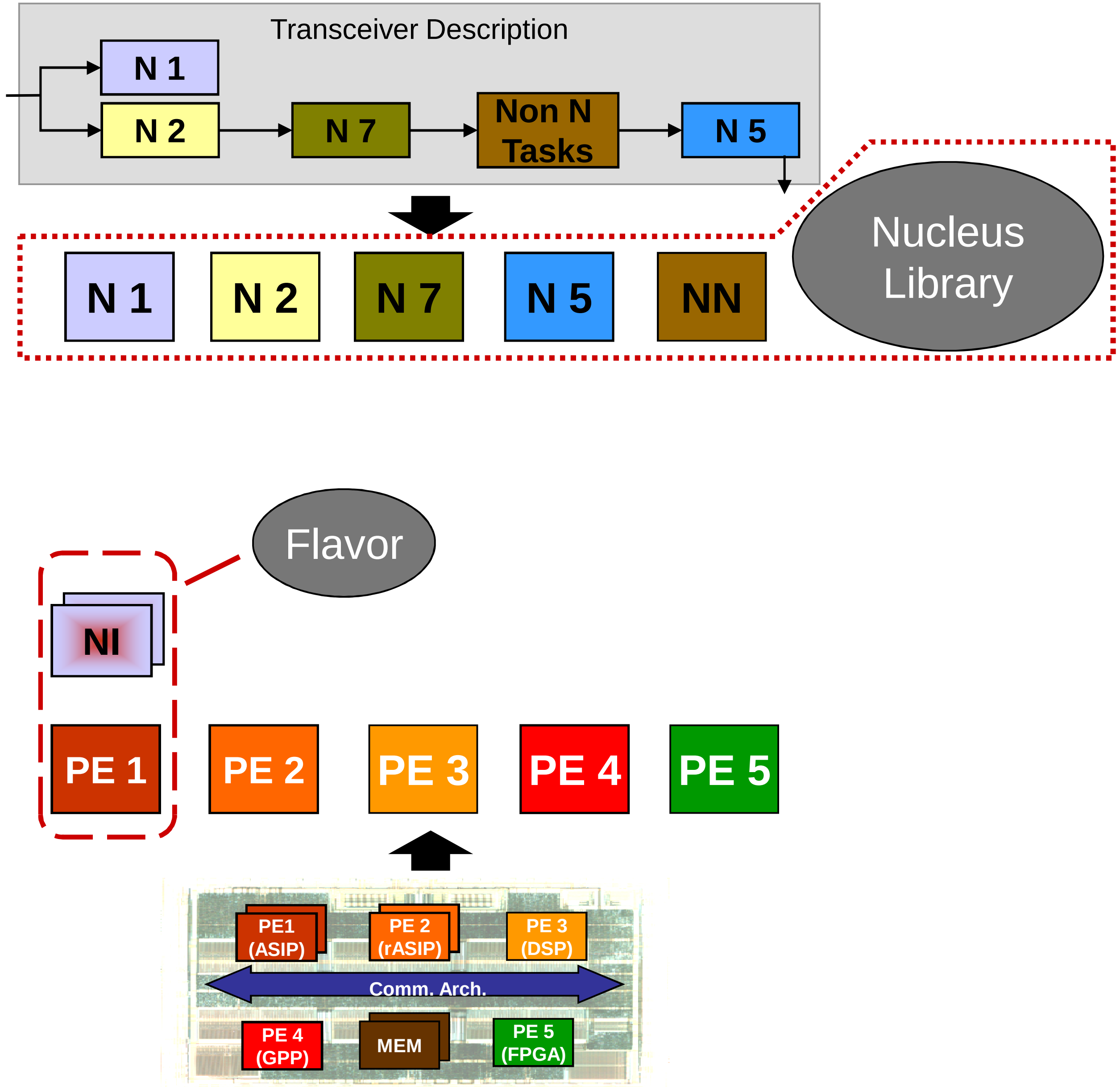
Nucleus Methodology

Transceiver Description

Nuclei

PEs

HW Platform



Nucleus Methodology

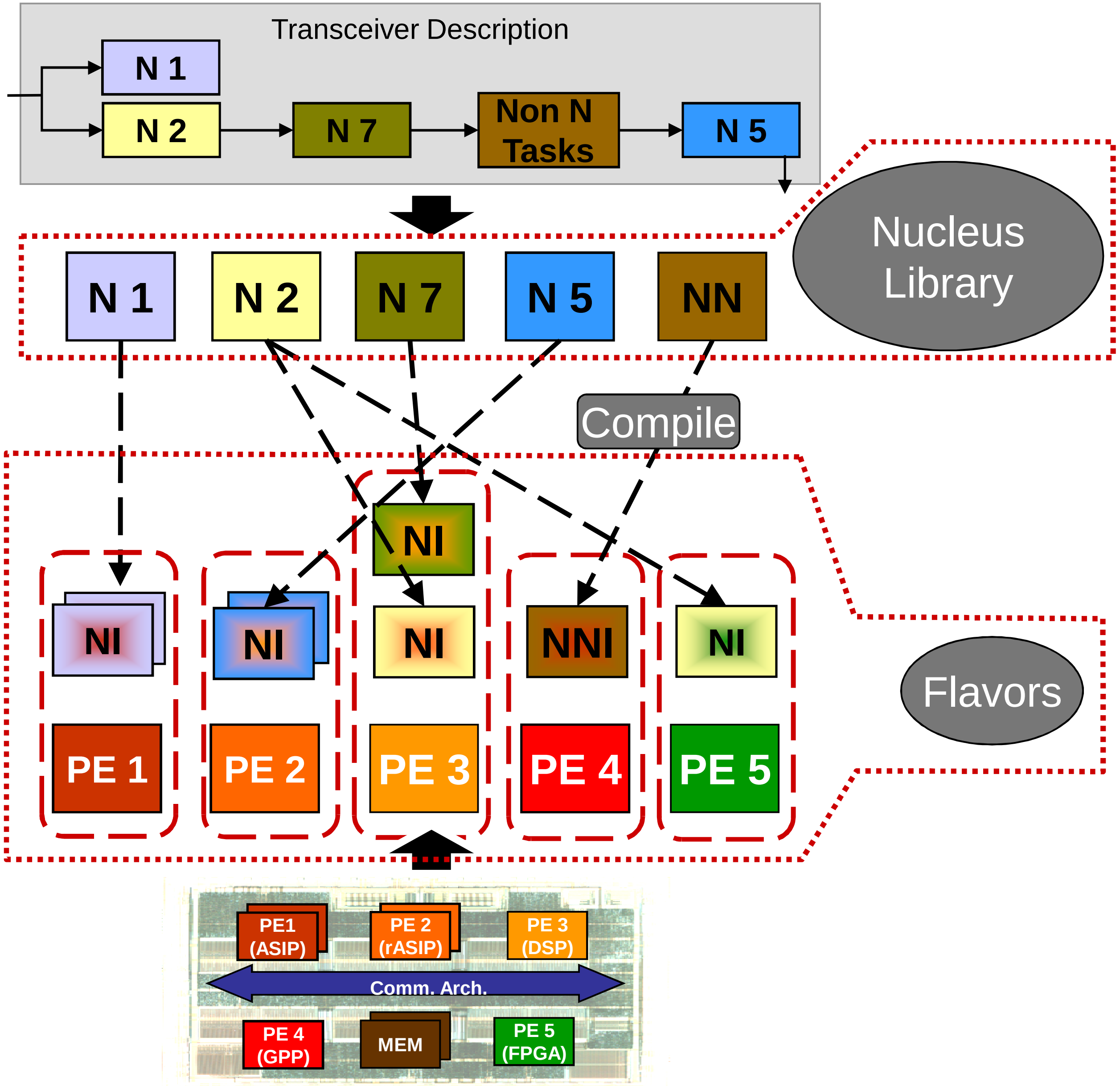
Transceiver Description

Nuclei

Mapping & Evaluation

Board Support Package

HW Platform



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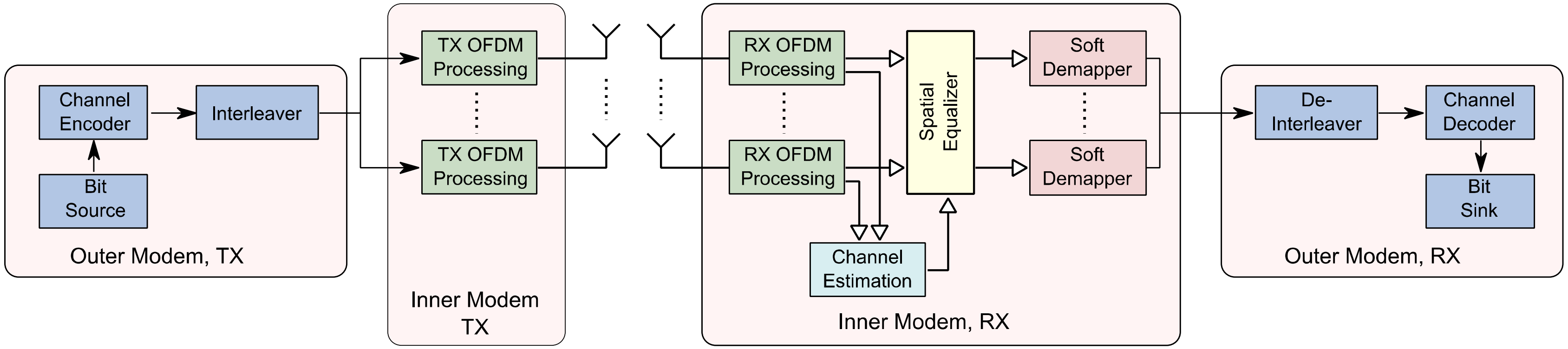
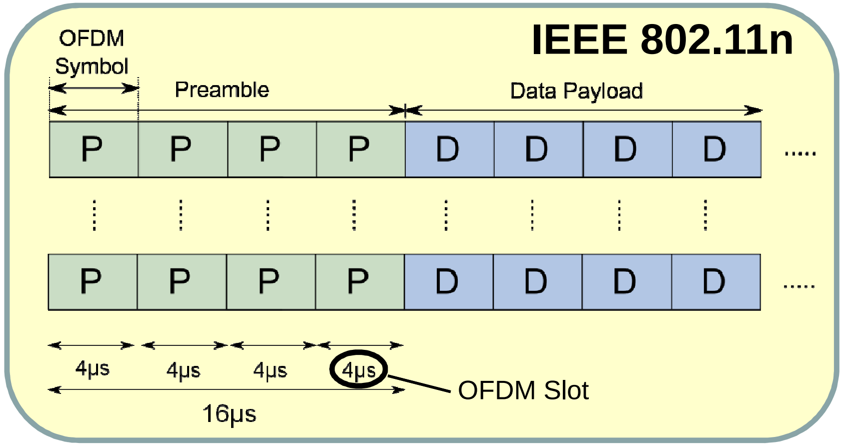
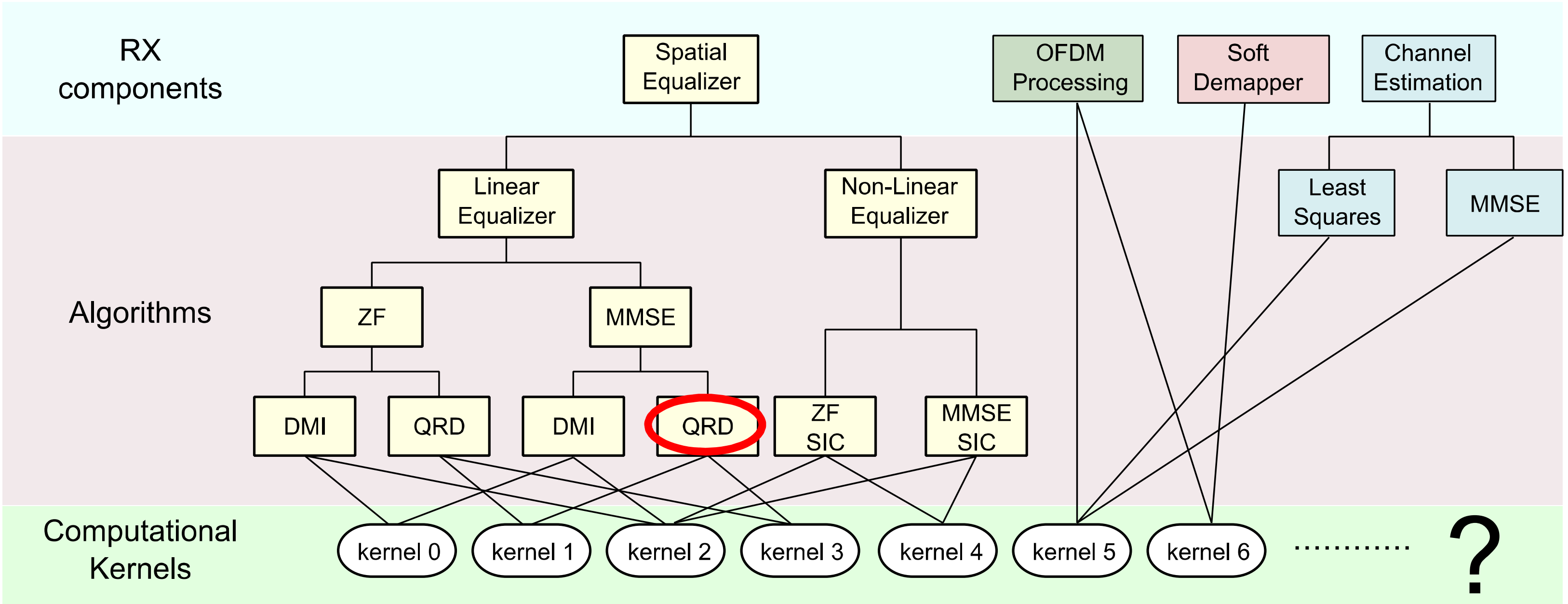


- **Outer Modem**
  - Channel (De-)coding
  - (De-)Interleaving
- **Inner Modem** (RX)
  - RX OFDM Processing
  - Channel Estimation
  - Spatial Equalizing: Mitigate channel impact on payload
  - Soft Demapping: Calculate soft bits (LLRs)
    BPSK, 4QAM, 16QAM



Nuclei Identification: Kernel Identification



- **Analyze different algorithmic choices within RX blocks**
  - Identify computational kernels
    - Recurring tasks
    - Operate on data with certain alignment
- **Build application as composition of kernels**

- **LMMSE MIMO Equalizer** with QRD
  - Basic transmission equation

$$\mathbf{y} = \mathbf{H}\mathbf{x} + \mathbf{n}$$

  - Linear MMSE equalization

$$\hat{\mathbf{x}} = \mathbf{G}\mathbf{y}, \quad \mathbf{G} = \left(\hat{\mathbf{H}}^{\mathbf{H}}\hat{\mathbf{H}} + \frac{\sigma_n^2}{E_s}\mathbf{I}\right)^{-1}\hat{\mathbf{H}}^{\mathbf{H}}$$

  - Regularized QRD

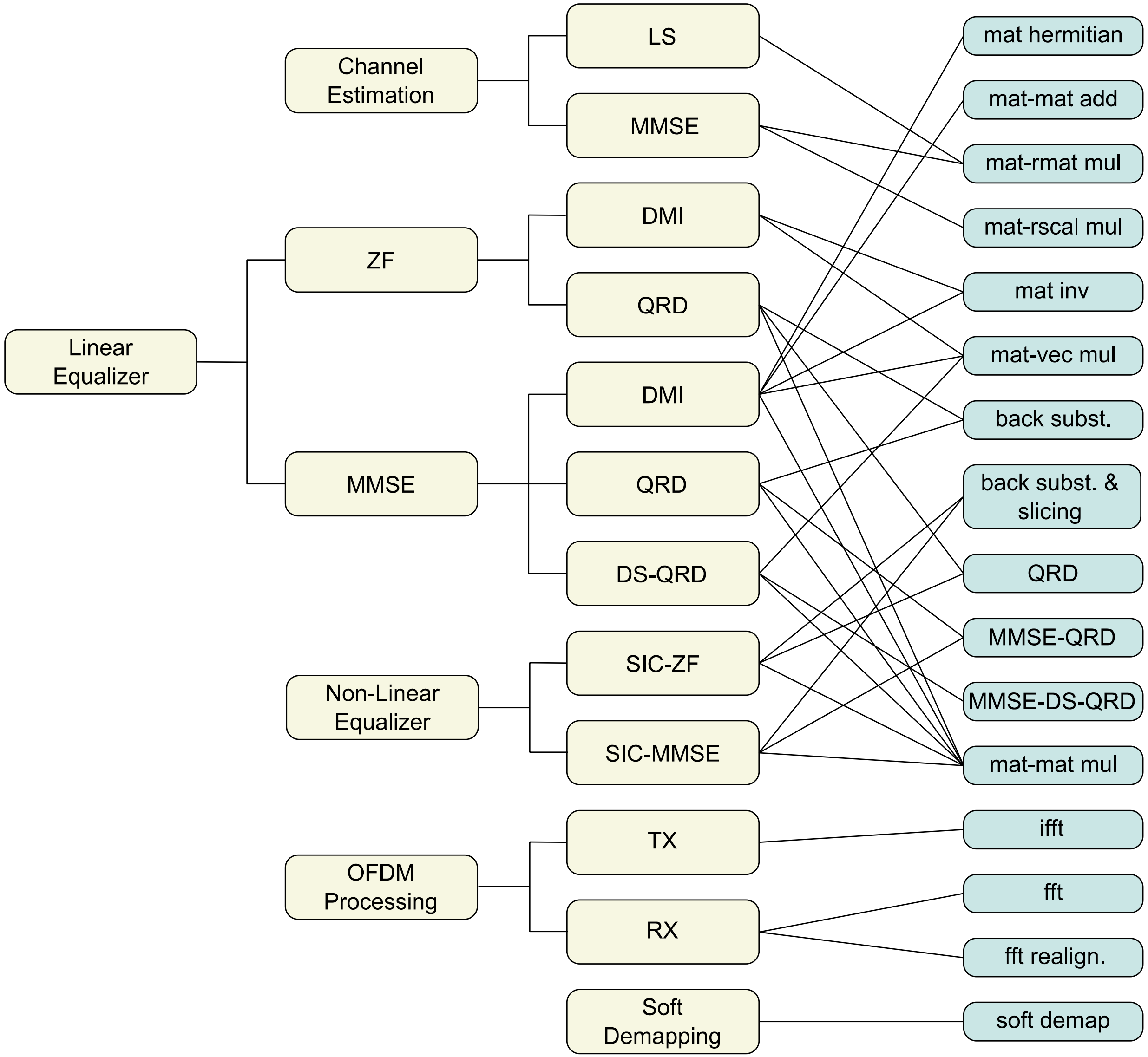
$$\overline{\mathbf{H}} = \begin{pmatrix} \hat{\mathbf{H}} \\ \frac{\sigma_n}{\sqrt{E_s}}\mathbf{I} \end{pmatrix} = \begin{pmatrix} \mathbf{Q}_{\mathbf{a}} \\ \mathbf{Q}_{\mathbf{b}} \end{pmatrix}\mathbf{R}$$

  - Rewrite **G** using $\mathbf{Q}_a$ and $\mathbf{Q}_b$

$$\mathbf{G} = \frac{\sqrt{E_s}}{\sigma_n}\mathbf{Q}_{\mathbf{b}}\mathbf{Q}_{\mathbf{a}}^{\mathbf{H}}$$

- **Computational Kernels**
  - Regularized QR decomposition
  - Matrix-matrix multiplication
  - Matrix-vector multiplication

Nuclei Identification: Kernel Overview



- **Application variants consist of a few kernels only!**

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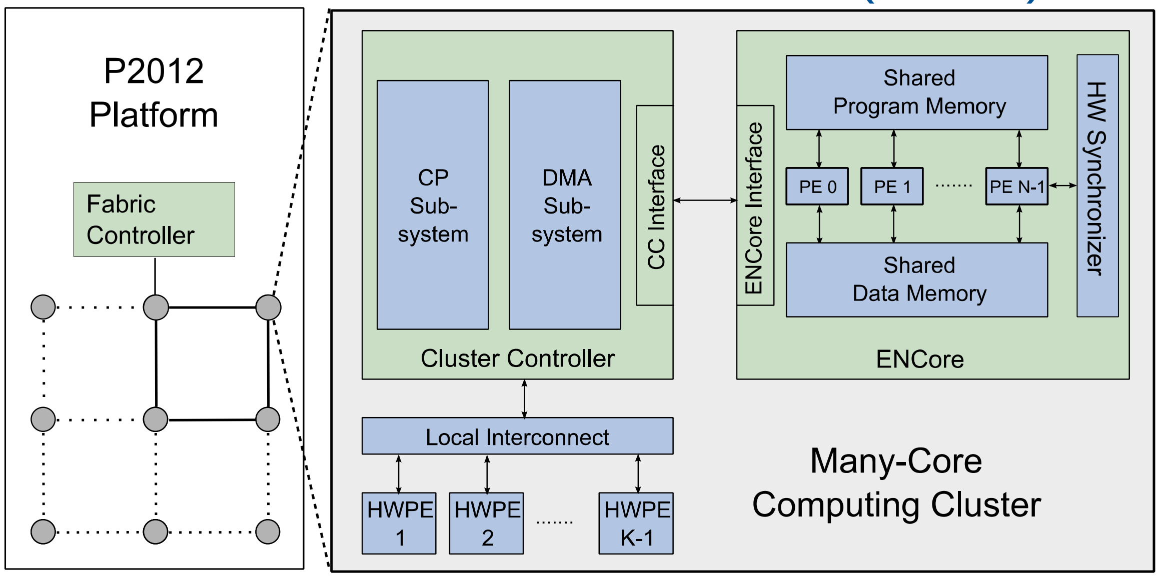
- **SoC platform with maximum of 32 clusters**
- **One cluster provides**
  - Max. 16 RISC cores (STxP70) @ 600MHz
  - VECx vector extension (SIMD)
    - 128 bit vector registers
    - **8x16 bit** or 4x32 bit operations
  - Hardware synchronizer for inter-core signaling
  - Interface for hardware accelerators (ASICs)



Application Implementation: Kernel Overview

	System Operation	2x2 cycles	2x2 time (μs)	4x4 cycles	4x4 time (μs)
	Matrix/Vector Operations				
1	mat-mat add	13	0.022	23	0.038
2	mat hermitian	26	0.043	90	0.150
3	mat-rscal mul	26	0.043	45	0.075
4	mat-vec mul	44	0.073	70	0.117
5	mat-mat mul	102	0.170	301	0.502
6	mat-rmat mul	74	0.123	205	0.342
7	mat-mat mul 8vm2[1]	218	0.363	503	0.838
8	mat inv	385	0.642	1,328	2.213
9	tri mat inv	43	0.072	278	0.463
10	qrd	595	0.992	1,683	2.805
11	qrd regularized	702	1.170	1,622	2.703
12	ds-qrd-regularized	889	1.482	2,264	3.773
13	back subst.	954	1.590	2,106	3.510
14	back subst. slicing	1,170	1.950	2,538	4.230
	OFDM slot wise operations				
15	bpsk soft demap	329	0.548	658	1.097
16	4qam soft demap	658	1.097	1,316	2.193
17	16qam soft demap	857	1.428	1,705	2.842
18	fft	1,774	2.957	3,548	5.913
19	fft mem realign	2,052	3.420	4,084	6.838
20	ifft	2,028	3.380	4,056	6.760

- **For 2x2 and 4x4 MIMO use case**
  - **Cycles for execution on single STxP70 processor core including VECX unit**
  - **Corresponding time for 600MHz clock frequency**

- **In the range of …**
  - **Competing solutions**
  - **IEEE 802.11n real time (4µs per OFDM slot)**

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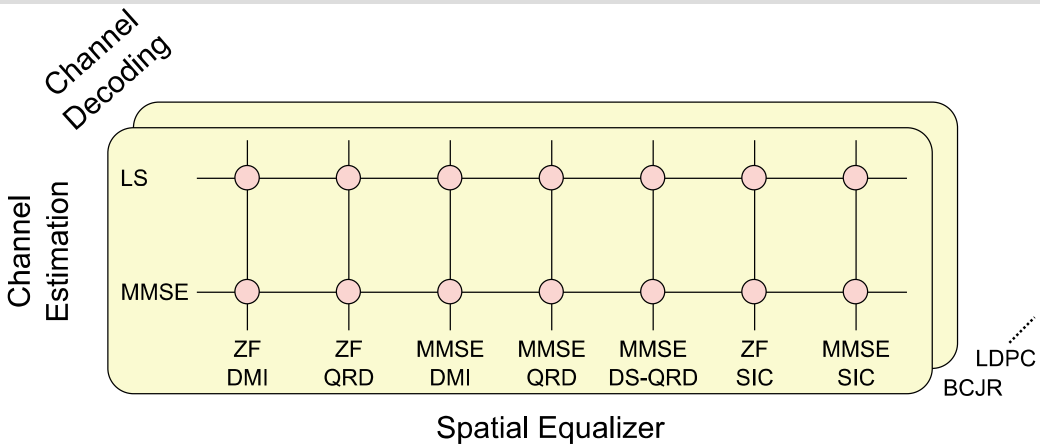
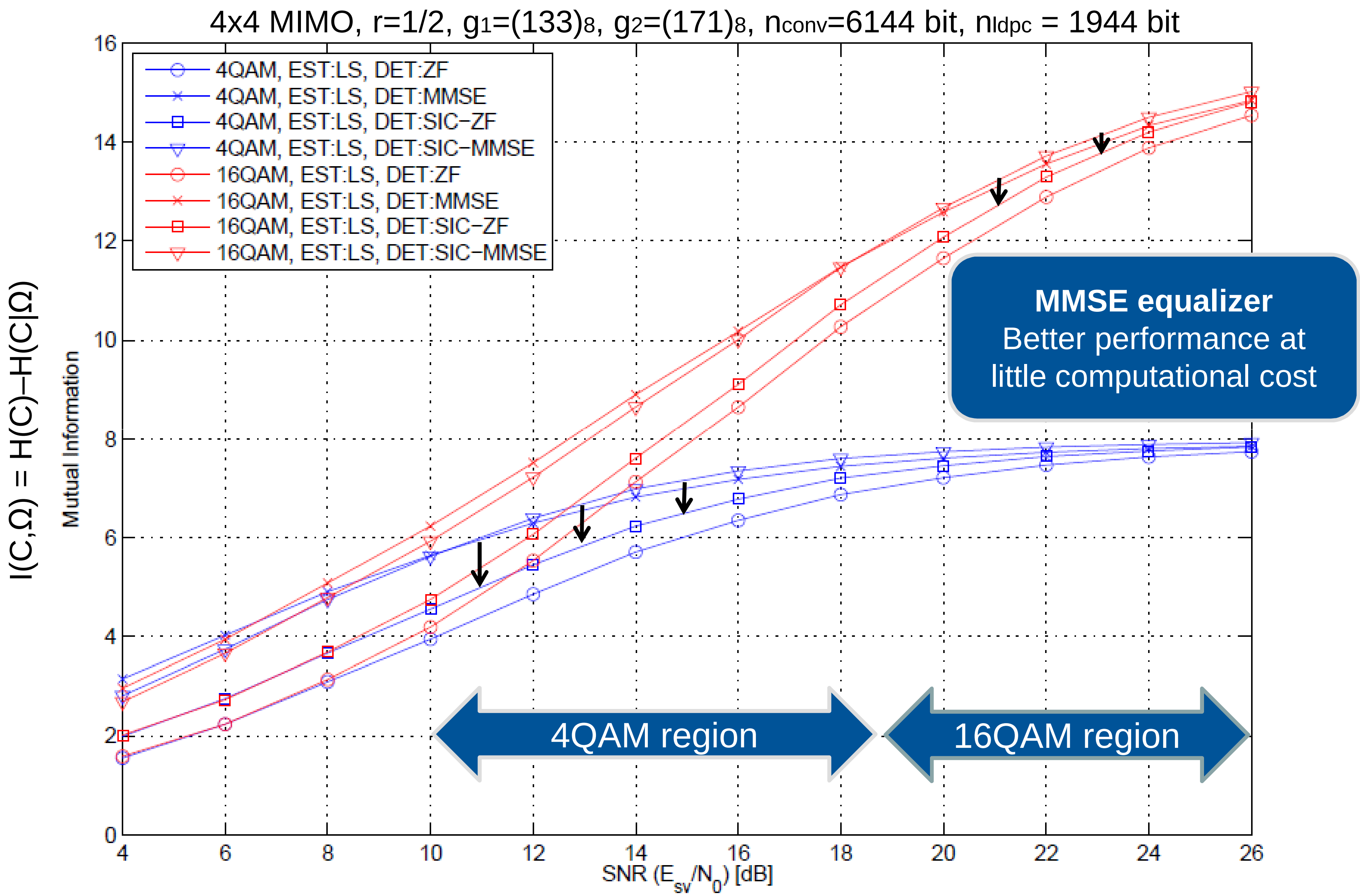
Algorithm Performance Evaluation: Investigated Algorithmic Choices

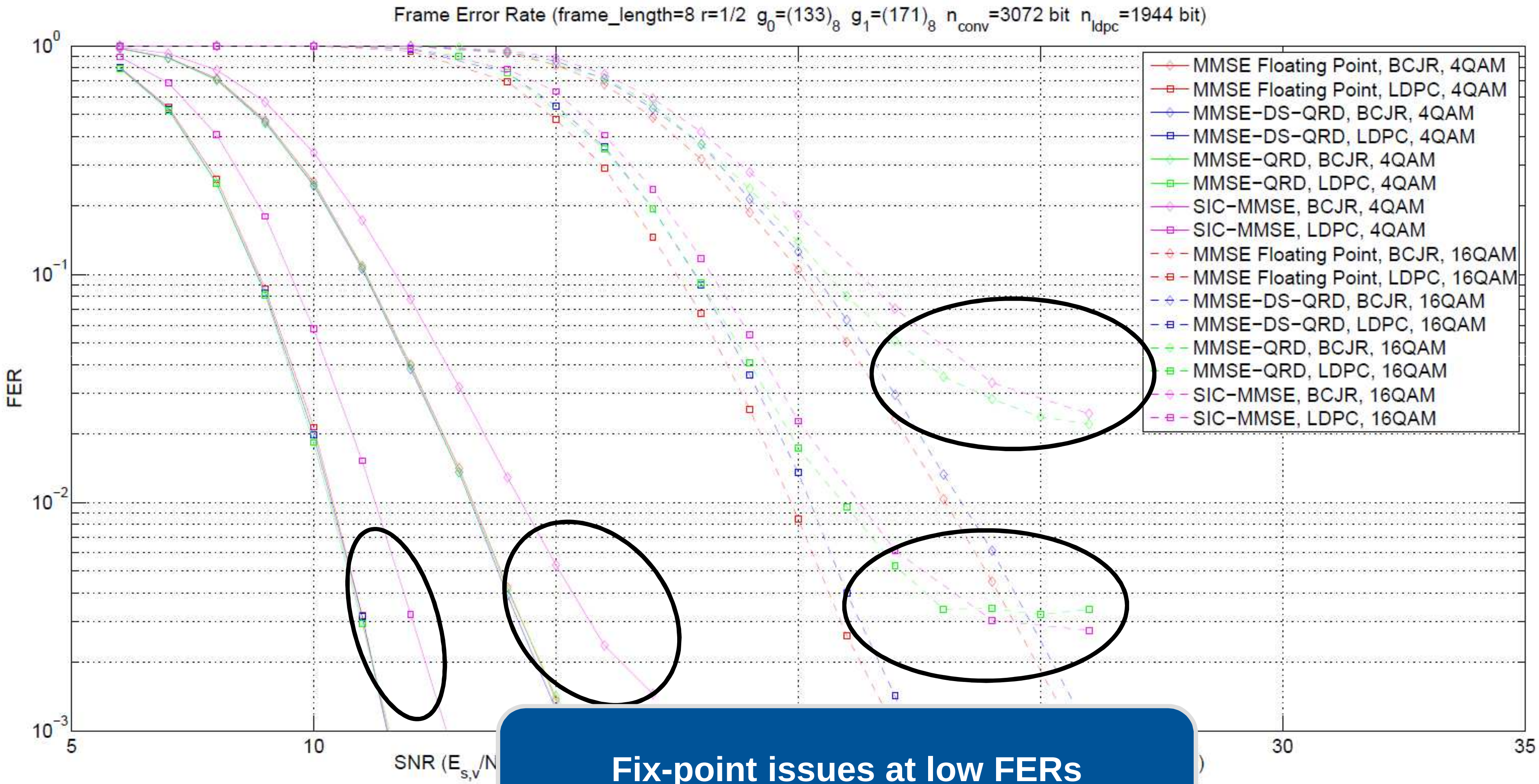


- **Wide variety of algorithms is implemented**
  - Channel Estimation, Spatial Equalizer, Channel Coding
- **Determine superior choice by error correction performance**
- **Channel simulation**
  - Fading: i.i.d. Rayleigh Fading
  - Power delay profile: Exponential 20dB drop along 150ns
  - Noise: AWGN
  - 4x4 MIMO system

Algorithm Performance Evaluation: ZF vs. MMSE MIMO Equalization



Frame Error Rate of 4x4 MIMO System (Short Frames)



Fix-point issues at low FERs when using MMSE-QRD, SIC-MMSE

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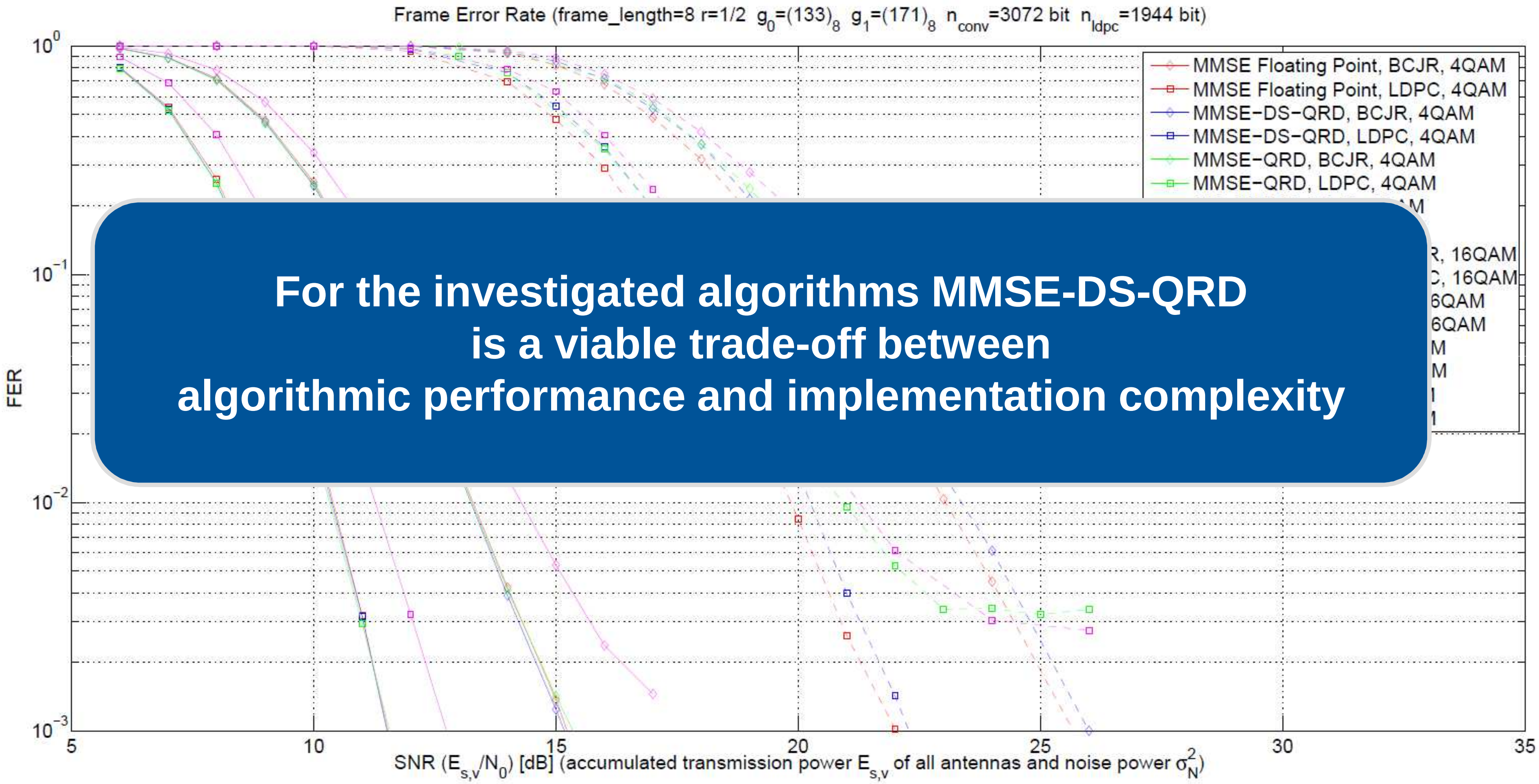
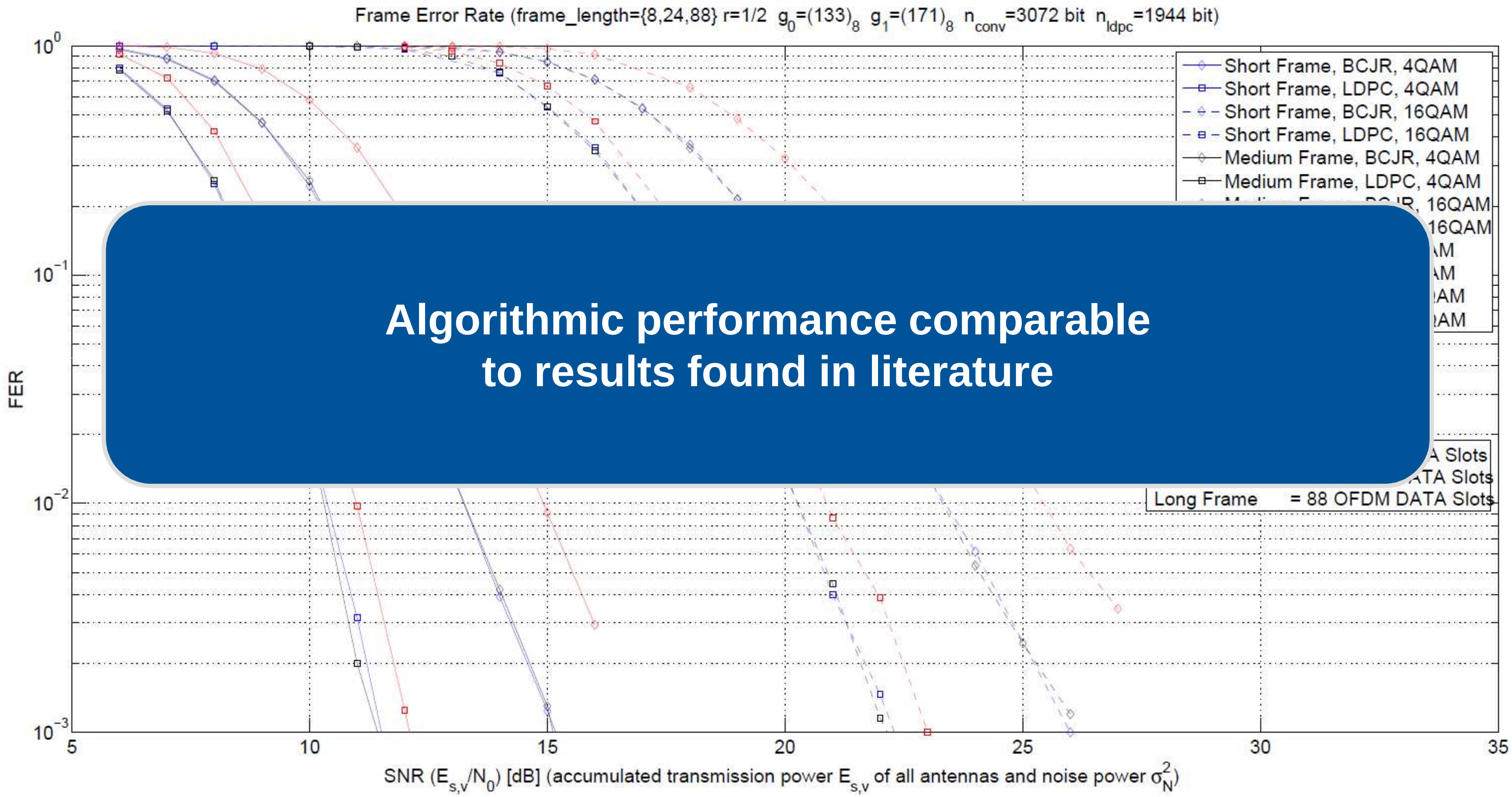
Frame Error Rate of 4x4 MIMO System (Short Frames)



For the investigated algorithms MMSE-DS-QRD
is a viable trade-off between
algorithmic performance and implementation complexity

Frame Error Rate of 4x4 MIMO System for different Frame Sizes



Algorithmic performance comparable to results found in literature

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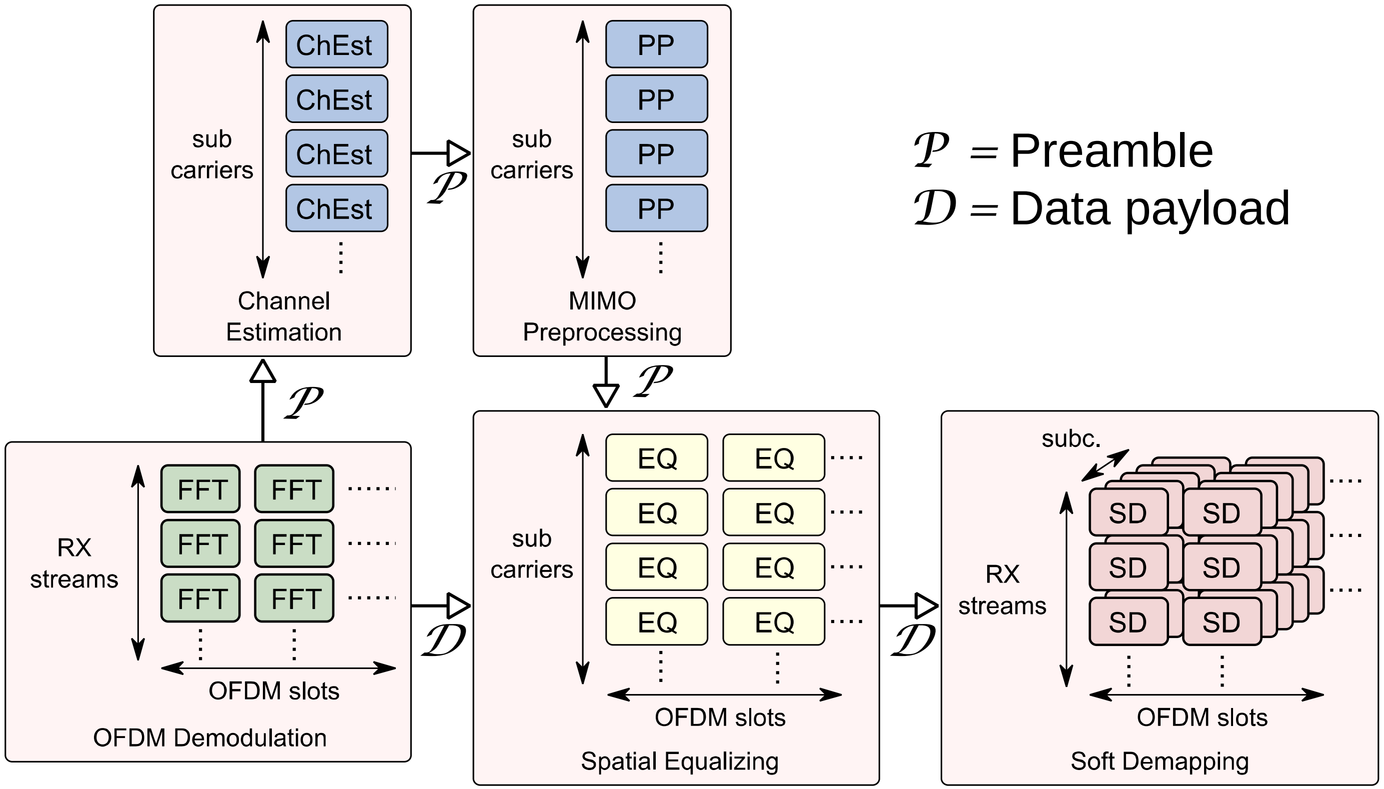
- **Parallelizable dimensions of OFDM receiver application**
  - Space (RX antennas)
  - Frequency (subcarriers)
  - Time (OFDM slots)

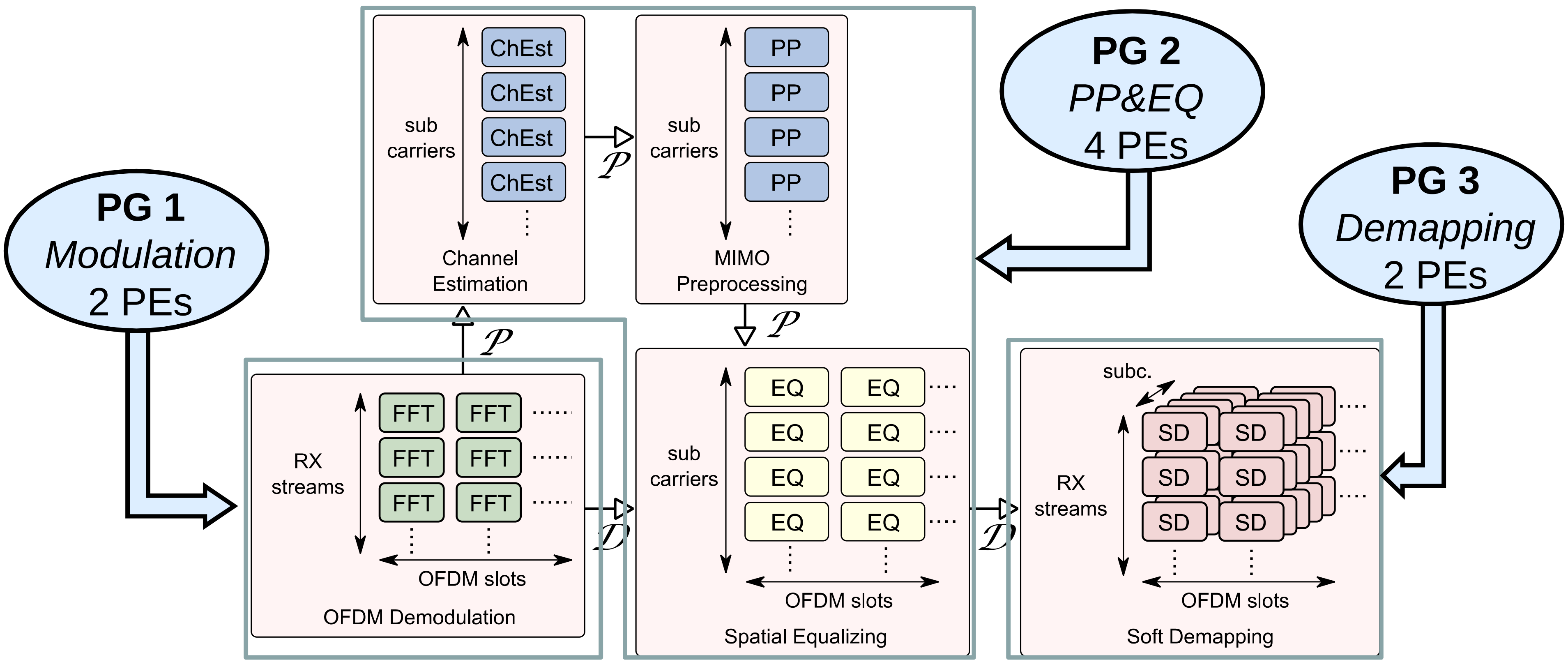


Application-to-Platform Mapping: Assign Cores to PGs

- **Given**: Single core timing requirements
- **Goal**: Assign cores to match real time constraints (4µs per slot)

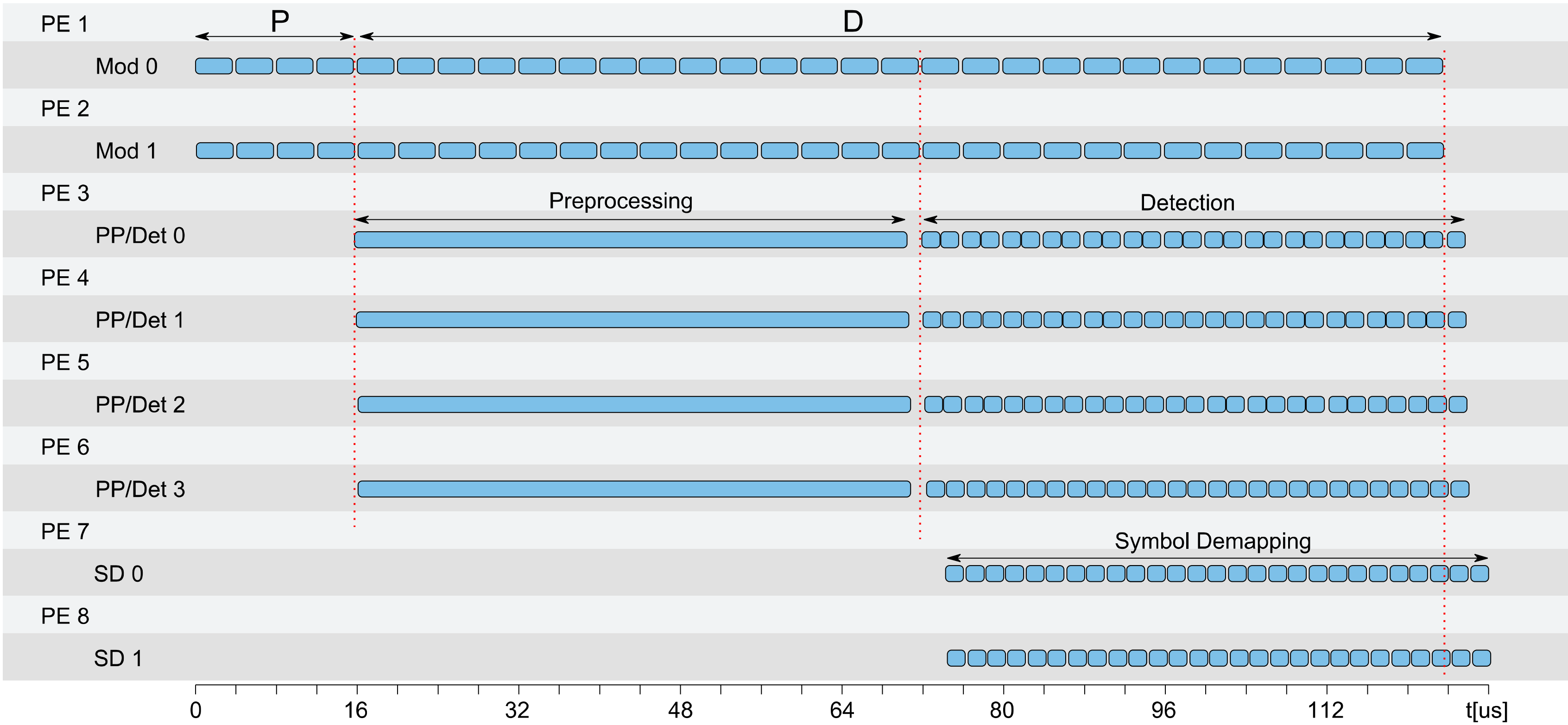
Task	time (us)	#cores
Preprocessing (per OFDM frame)		
LS Channel Estimation	17.47	4
Equalizer Preprocessing	215.31	4
Actual Processing (per OFDM slot)		
OFDM Demodulation (mem. realign)	6.83	2
Equalizer (Actual Detection)	6.08	4
Soft Demapping (16 QAM)	2.84	2

- **Final mapping**
  - Partitioning of components into processing groups
  - Number of cores per group
    - 8 cores enable real time



2PARMA: Occupation Graph

- Implementation on P2012 platform using 8 cores
- Minimum latency for 27 or more OFDM slots of data payload
- Latency = 8.2µs
- IEEE 802.11n allows 16µs (including MAC layer)



Thank you for your attention !

Any questions?

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