



# **Dynamic Reconfiguration Technologies Based on FPGA in Software Defined Radio System**

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# Outline

- Motivation and Objective
- Reconfiguration Technologies : Dynamic Reconfigurable Ports and Partial Reconfiguration.
- Multiple Standards Analysis : Modulation and Digital Front End parts of LTE, WiMAX and WCDMA standards
- Hierarchical Design Methodology
- Results and Comparisons
- Conclusion

# Motivation

- Software Defined Radio can accommodate various standards and services
- Partial Reconfiguration is a promising technology which could increase hardware reuseability therefore reduce hardware cost and has commonalities with SDR
- For some cases, PR can work with Dynamic Reconfigurable Ports (DRP) technology which could lead to a less complex and lower cost SDR architecture.

# Objective

- Implement the key components e.g. Modulation and Digital Front End with PR to support multiple communication standards such as WCDMA WiMAX and 3GPP LTE
- Integrate these components into a single FPGA device with PR and DRP technologies to build a SDR system with less complex and lower cost architecture, while maintaining a high degree of design and function switching flexibility.

# Partial Reconfiguration Technology

The Partial Reconfiguration is such a technology that allows multiple design modules to time-share physical resources. Reconfigurable modules can be swapped on the fly and other parts the remain operation

## Advantages:

- Increase hardware reuseability
- Reduce hardware size and cost

## Limitation:

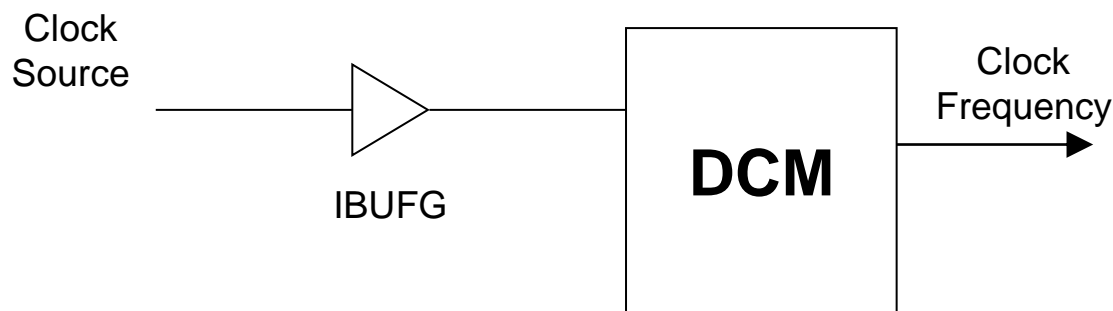
The clock frequency could not be reconfigured by PR as the Digital Clock Manager (DCM) are not allowed to place in the reconfigurable logic



# Dynamic Reconfigurable Ports Technology

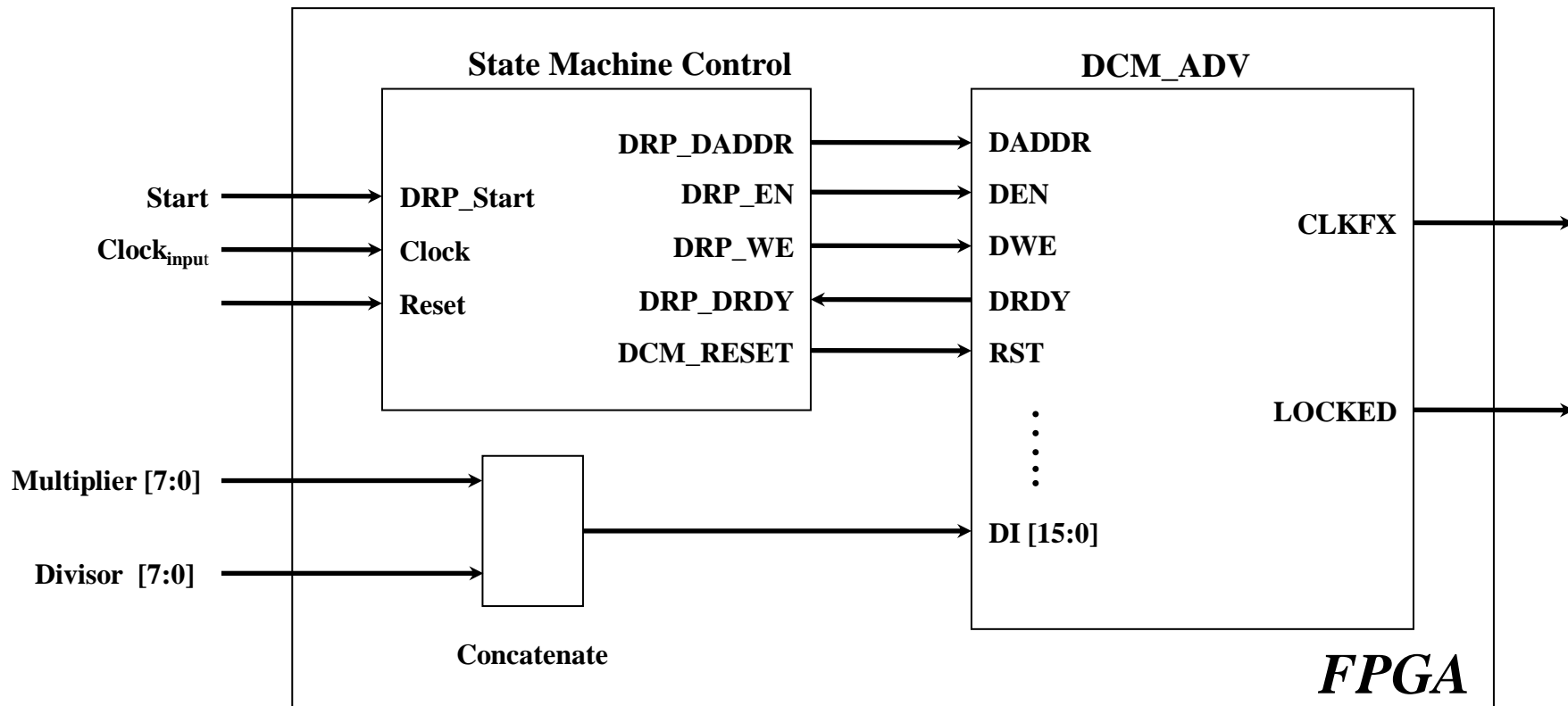
Digital Clock Managers (DCMs) : A hardware resource on FPGA to deal with the clock managements

- Eliminate clock skew
- Shift phase
- Synthesize a desired clock frequency





# Dynamic Reconfigurable Ports Technology

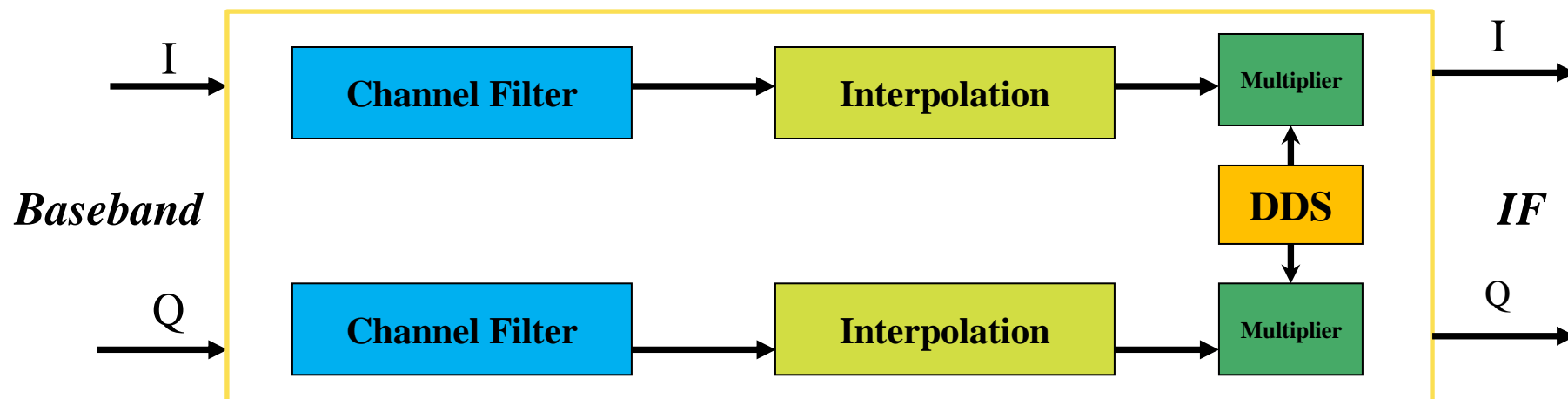


# Multiple Communication Standards Analysis

## ➤ Modulation Analysis

Standards	Mapper	OFDM		OVSF
		FFT Size	CP Length	Spreading Factor
LTE 5/10 MHz	QPSK 16QAM 64 QAM	512, 1024	80,72 and 40,36 samples	None
WiMAX 3.5/5/7/10 MHz	QPSK 16QAM 64 QAM	512, 1024	1/4, 1/8, 1/16, 1/32 of frame duration	None
WCDMA	QPSK	None	None	4,8, 16,32, 64, 128, 256, 512

## ➤ Digital Front End Analysis





# Multiple Communication Standards Analysis

Design Bandwidth	Input Sample Rate (Msps)	IF (MHz)	System Clock (MHz)
LTE 5 MHz	7.68	61.44	245.76
LTE 10 MHz	15.36	61.44	245.76
WCDMA	3.84	61.44	245.76
WiMAX 3.5 MHz	4	64	256
WiMAX 5 MHz	5.6	44.8	179.2
WiMAX 7 MHz	8	64	256
WiMAX 10 MHz	11.2	44.8	179.2

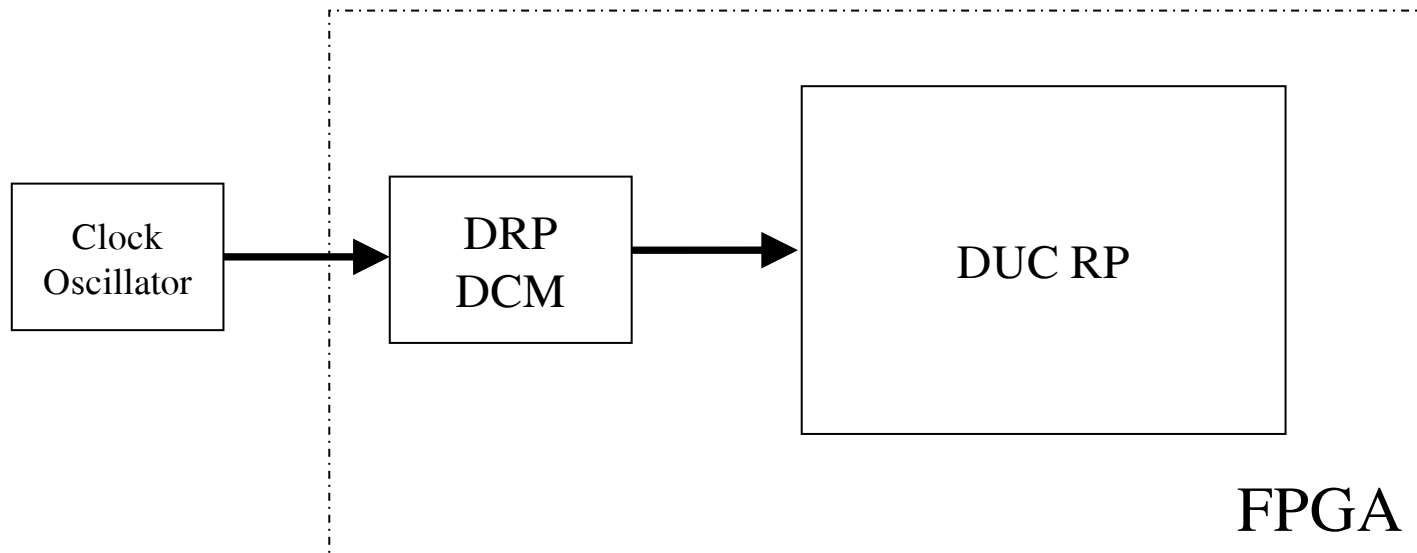
## Note:

- Three standards and 7 modes
- System Clock of 4 times of the IF Sample Rate
- Three different clock frequencies are required: 245.76 MHz, 256 MHz and 179.2 MHz

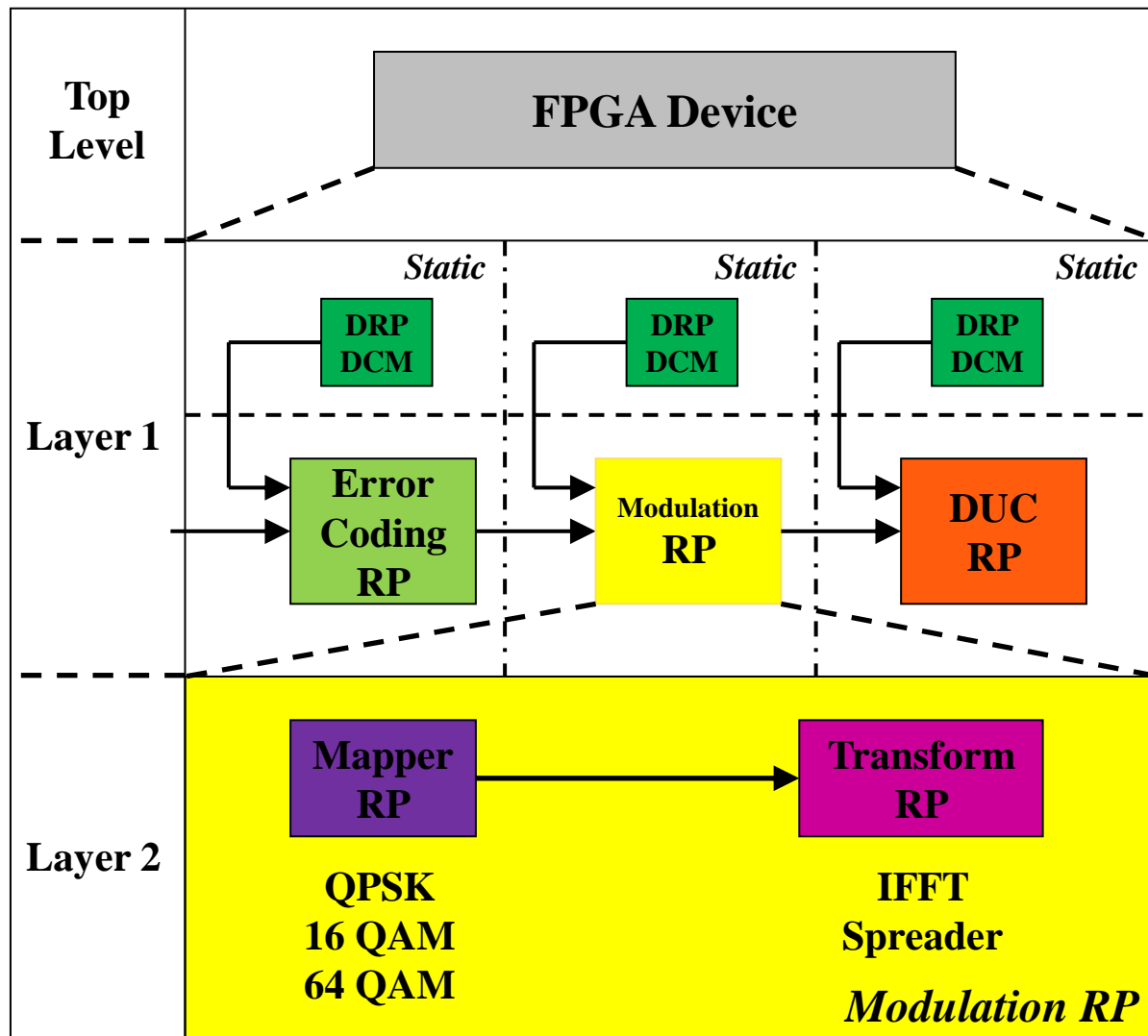


# Combination of dynamic reconfiguration technologies

- Waveforms switching means not only changing functions but also changing the clock frequency of the function
- PR is insufficient to implement all of the switching functions in isolation
- The DCM with DRP architecture is able to control for the Reconfigurable Partition



# Hierarchical Design Methodology

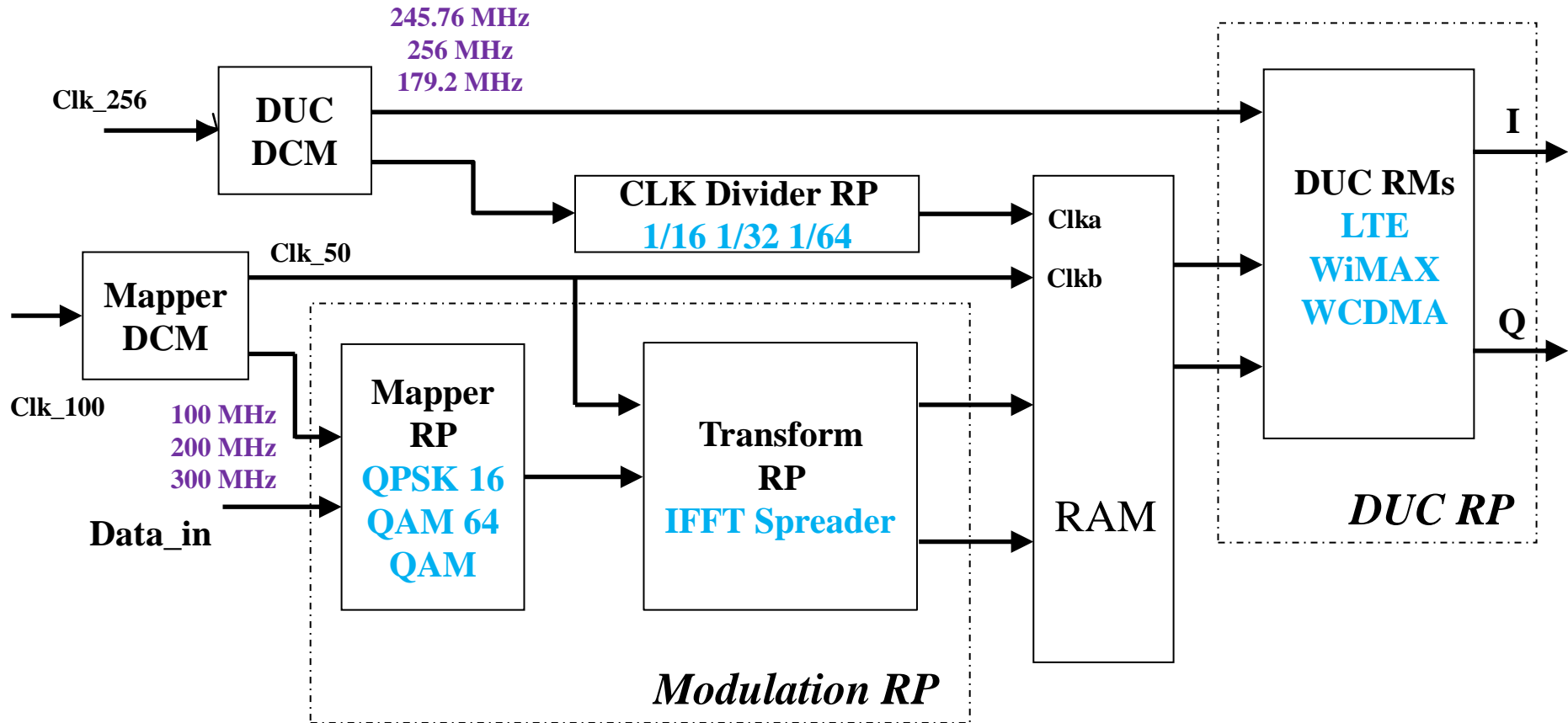


## Advantages:

- PR benefits
- High integration on a single FPGA
- Reconfigurable clock frequencies
- High degree of flexibility
- Easy to maintain and update

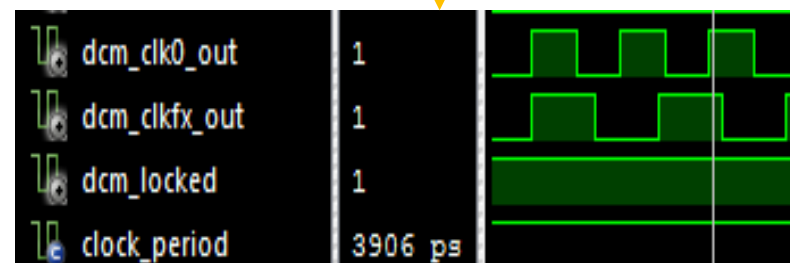
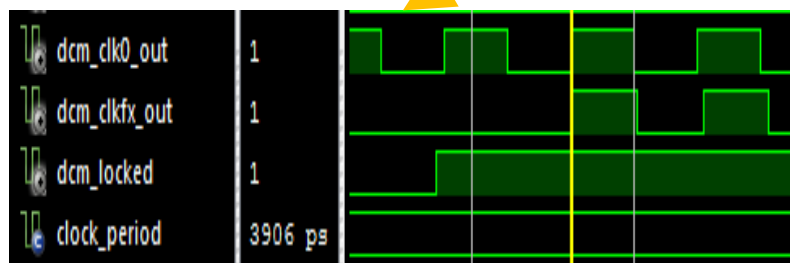
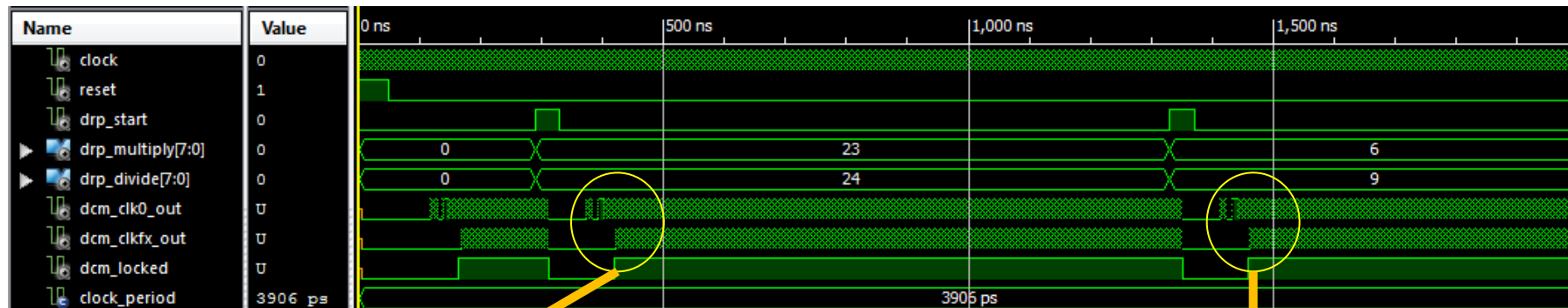


# Hierarchical Design Methodology





# Results: Post-Placed and Route Simulation



# Hardware Resource Utilization Results

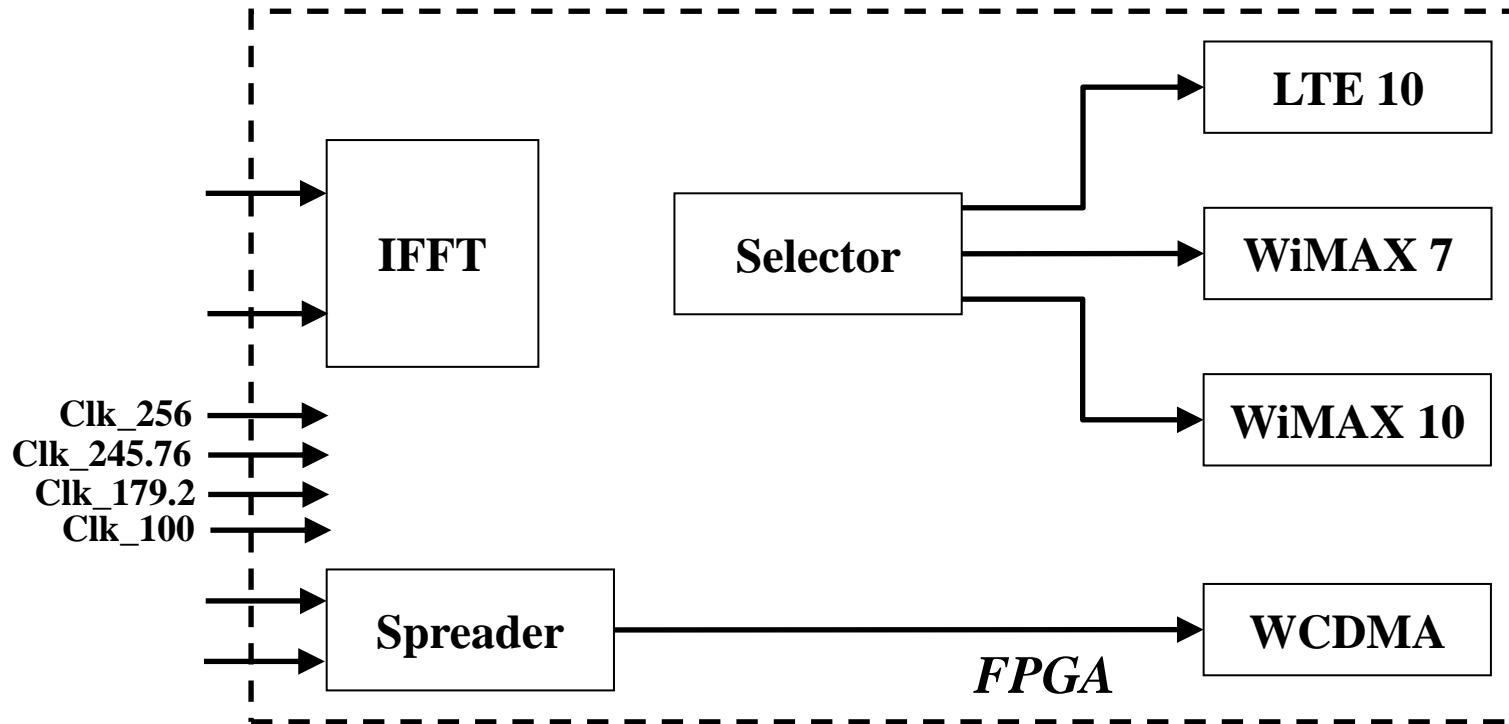
**Table 1: Without PR**

RP		LUTs	FFs	Slices	DSP4 8Es	RAMs	(MHz)
<b>DUC</b>	LTE 5	1504	2148	799	11	9	424.1
	LTE 10	1438	2004	872	14	9	355.6
	WCDMA	1493	2020	722	8	9	419.1
	WiMAX 3.5	1629	2223	869	14	9	386
	WiMAX 5	1474	2083	817	14	9	390.9
	WiMAX 7	1540	2194	878	17	9	312
	WiMAX 10	1449	2130	842	20	9	295.3
<b>Transform</b>	OFDM	3430	3570	1405	12	5	286.9
	Spreader	34	9	11	0	0	375.7

**Table 2: With PR & DRP**

RP		LUTs	FFs	Slices	DSP4 8Es	RAMs	(MHz)
<b>DUC</b>	LTE 5	1533	2005	543	11	9	336.2
	LTE 10	1455	1873	557	14	9	374.2
	WCDMA	1532	1899	533	8	9	273.8
	WiMAX 3.5	1663	2079	582	14	9	280.0
	WiMAX 5	1497	1964	554	14	9	269.3
	WiMAX 7	1565	2084	612	17	9	354.1
	WiMAX 10	1466	2014	604	20	9	374.0
<b>Transform</b>	OFDM	3442	3559	1193	12	5	275.6
	Spreader	45	9	12	0	0	188.0

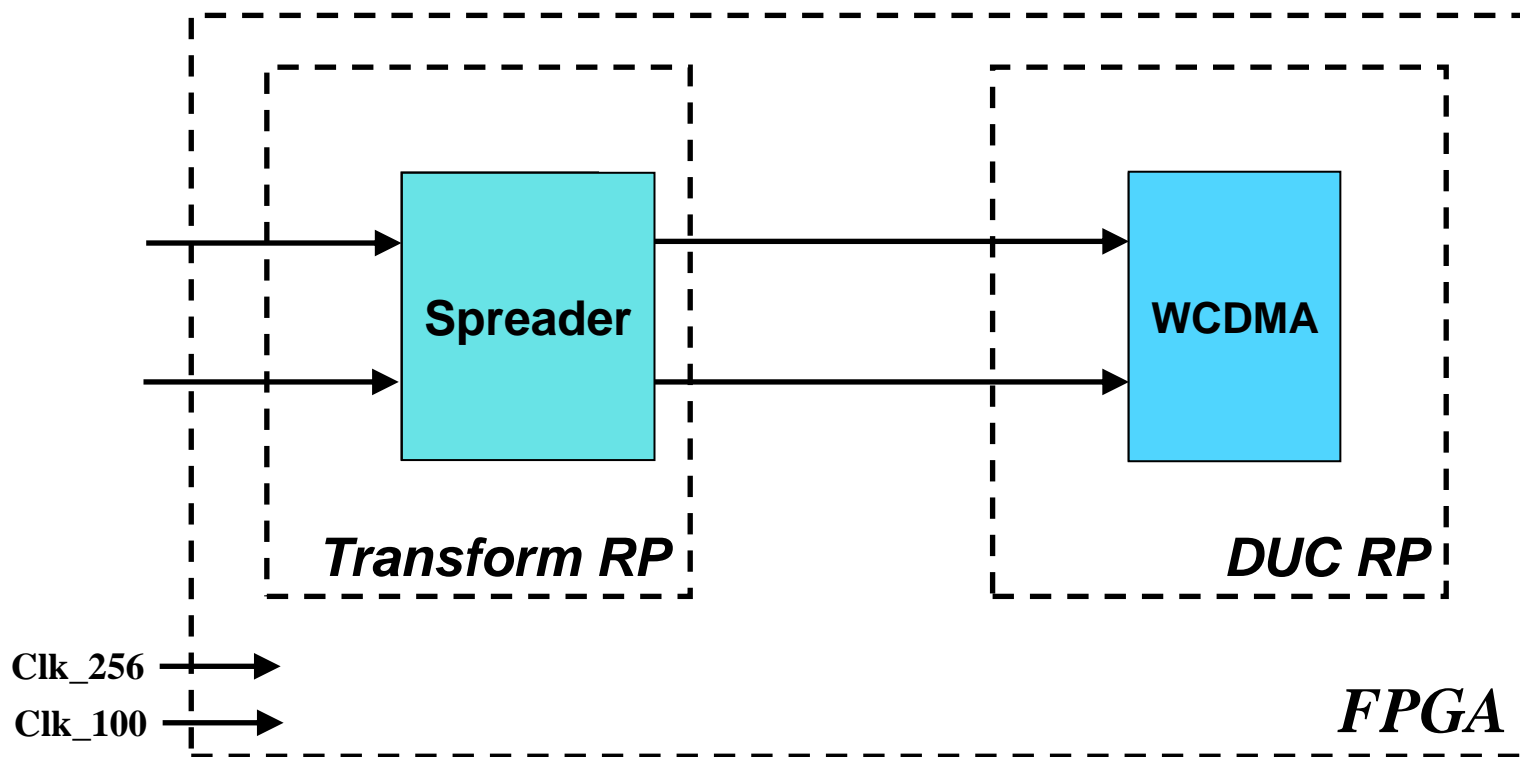
## Fix function FPGA Design to support multi-standards



Slices	DSP48Es	RAMs
4657	71	41



# PR & DRP Design Architecture

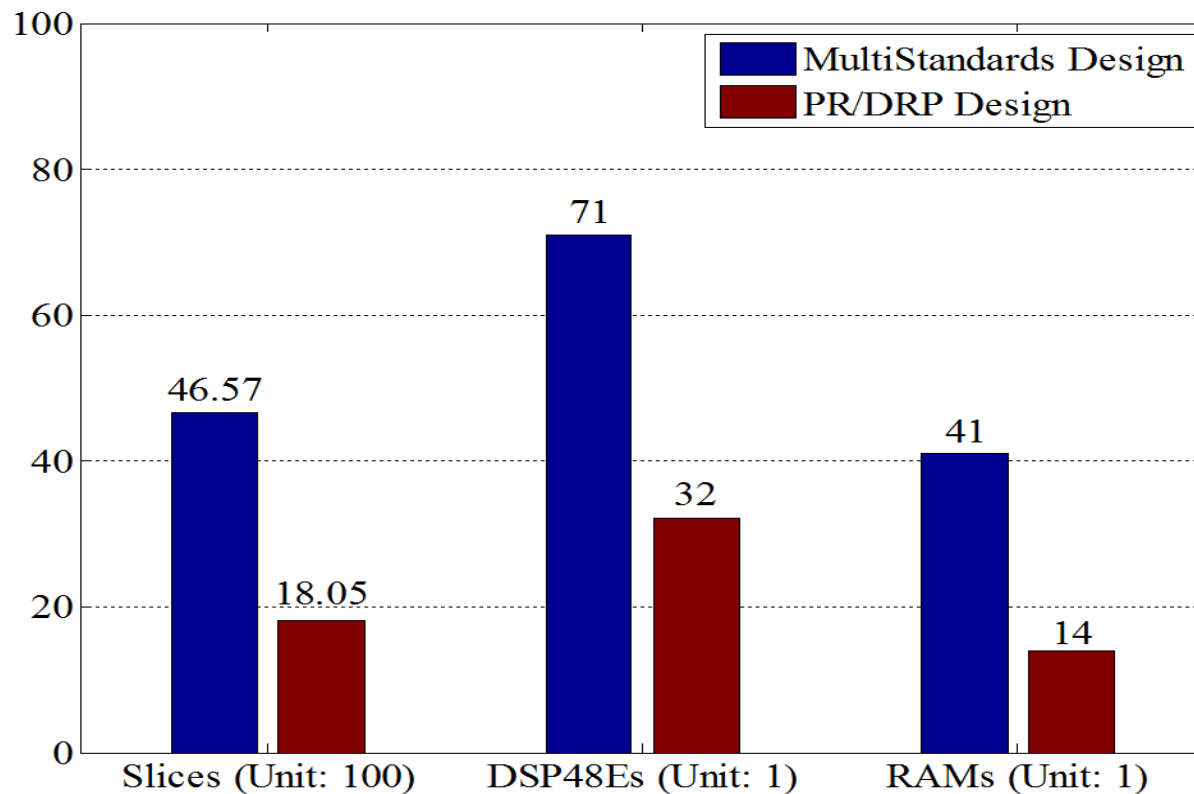


$$Resource = \max(\text{transform}(RP)) + \max(\text{DUC}(RP))$$

Slices	DSP48Es	RAMs
1805	32	14



# Results and Comparison



	Slices	DSP48Es	RAMs
Reduction	61.24%	54.93%	65.85%





# Conclusion

- Support Baseband and IF processing components
- Support multiple standards and modes
- High degree of design and function switching flexibility
- Reduction of 61.24%, 54.93% and 65.85% in respect of Slices, DSP48Es and RAMs
- Reduction of two oscillator inputs