Analog-to-Digital Conversion – the Bottleneck for SDR Frontends

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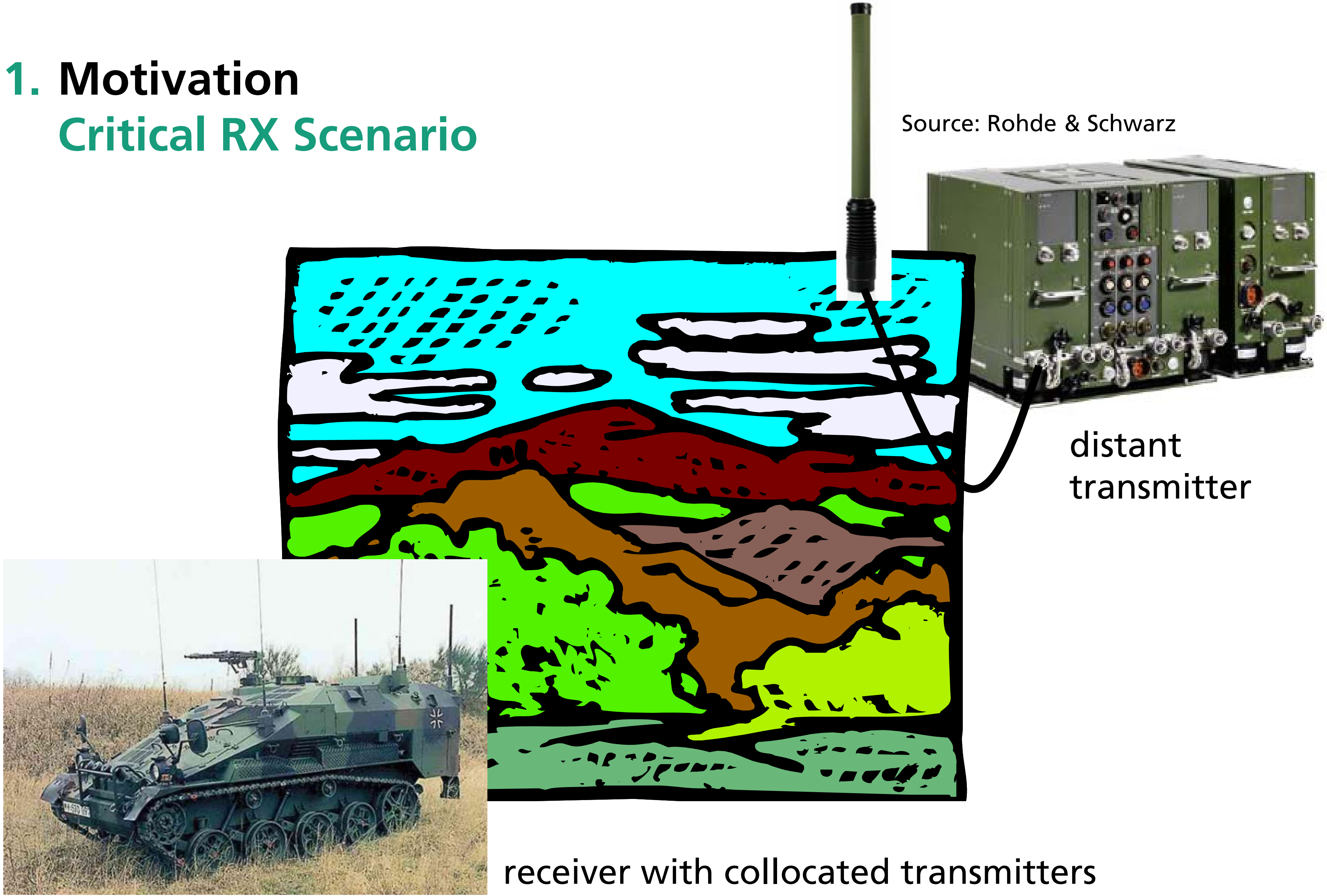
Overview

1. Motivation
2. Analog-to-digital conversion
    - Theory – ideal sampling and quantization
    - Non-ideal analog-to-digital conversion
    - ADC architectures and state-of-the-art
3. Dynamic range enhancement techniques
    - Automatic Gain control
    - Non-uniform quantization
    - Parallel ADCs: Time Interleaved ADCs and Signal Averaging
4. Conclusions

1. Motivation

Critical RX Scenario



Source: Rohde & Schwarz

distant transmitter

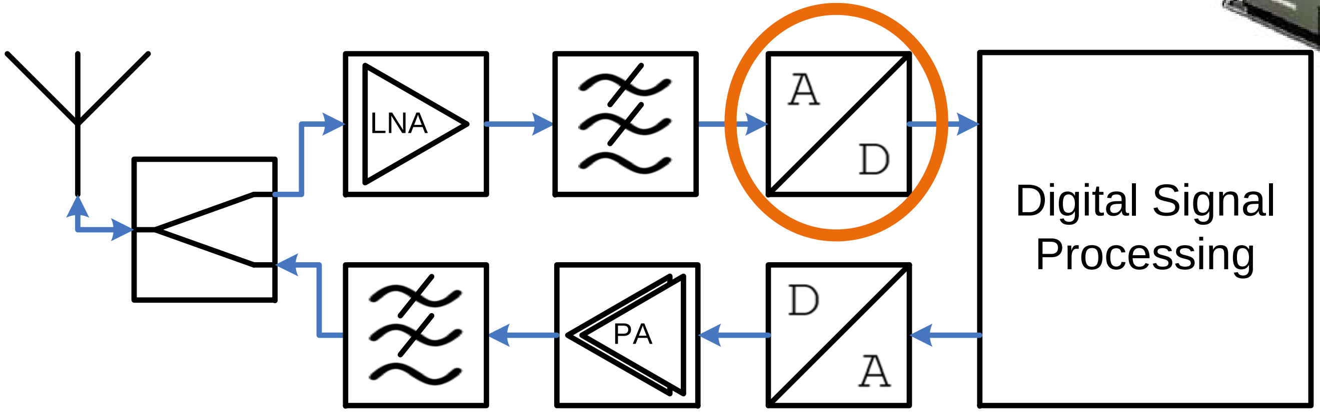
receiver with collocated transmitters

Source: www.deutschesheer.de

1. Motivation

Advantages of SDR Architectures

Software Radio architecture

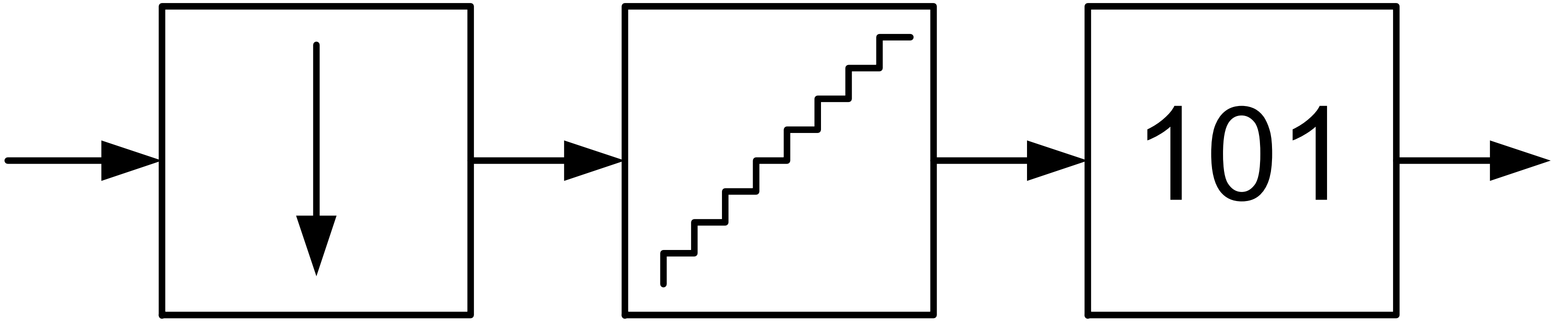


- SDR architecture gives multi standard capability => several waveforms running on one radio (e.g. for national and alliance communication)
- upgradeability => from legacy waveforms to upcoming waveforms
- flexible RF architecture (e.g. frequency range, bandwidth, fast hopping)
- => higher flexibility

2. Analog-to-Digital Conversion
Theory

Analog-to-digital conversion comprises three operations:

1) sampling, as a conversion from continuous time to discrete time
2) quantization, as a conversion from continuous values to discrete values
3) coding, generating a binary representation of the sampled value



2. Analog-to-Digital Conversion

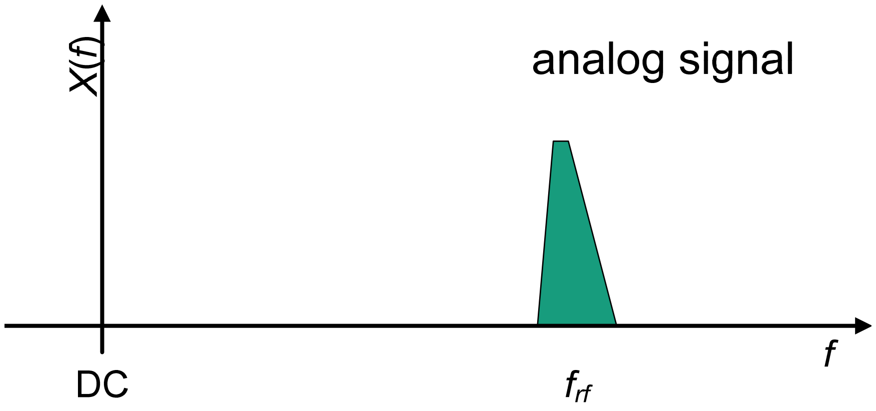
Ideal Sampling

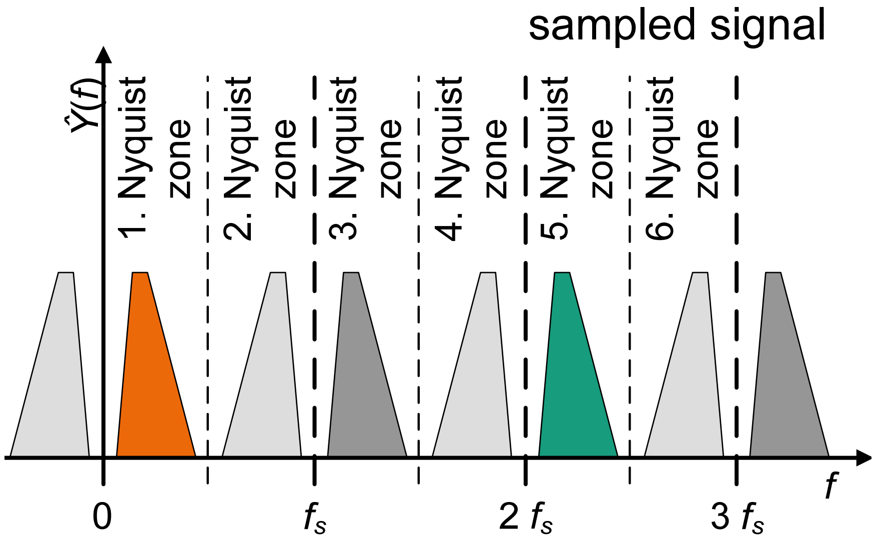
$$\hat{y}(t) = x(t) \cdot s_a(t) = x(t) \sum_{n=-\infty}^{\infty} \delta(t - nT)$$

$$s_a(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT) = \frac{1}{T} \sum_{n=-\infty}^{\infty} e^{jn\frac{2\pi}{T}t}$$

$$\hat{y}(t) = \frac{1}{T_S} \sum_{n=-\infty}^{\infty} x(t) e^{jn\frac{2\pi}{T_S}t}$$

$$\hat{Y}(f) = \frac{1}{T_S} \sum_{n=-\infty}^{\infty} X(f - nf_S)$$

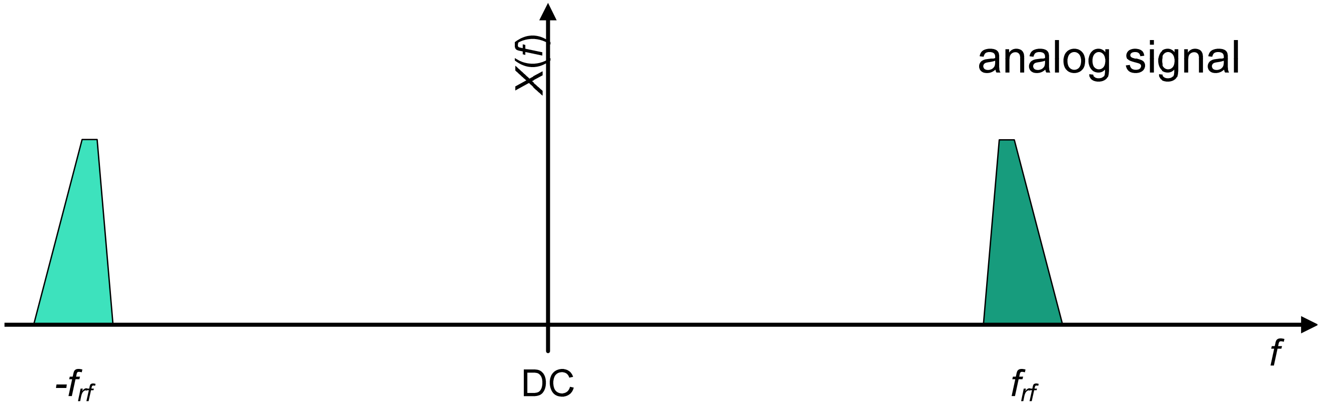


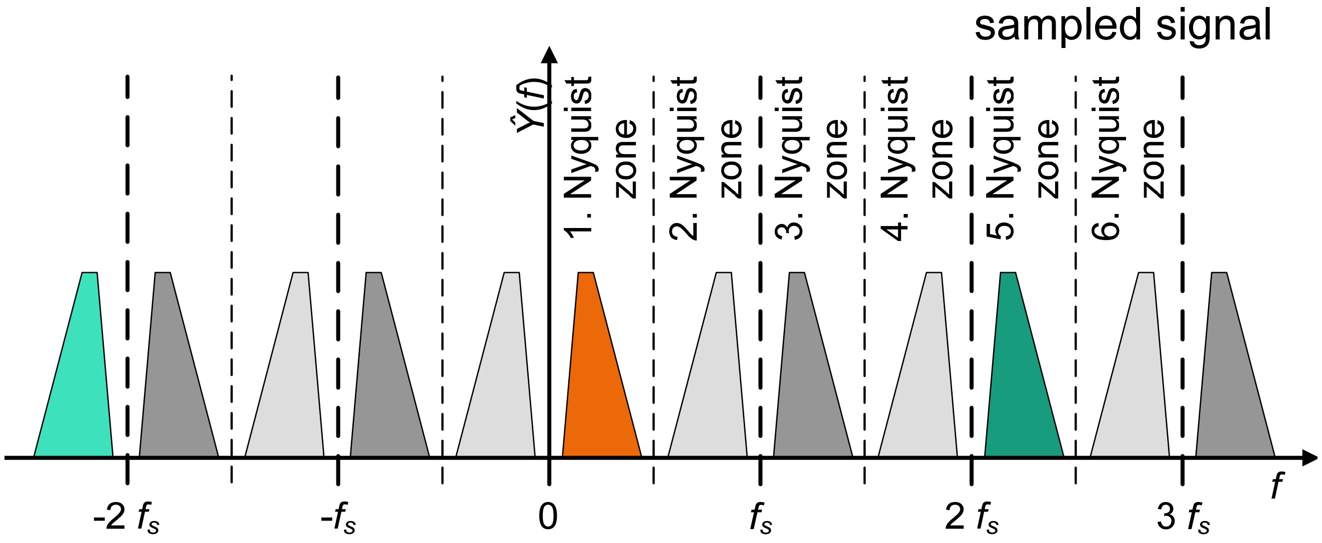


2. Analog-to-Digital Conversion

Ideal Sampling

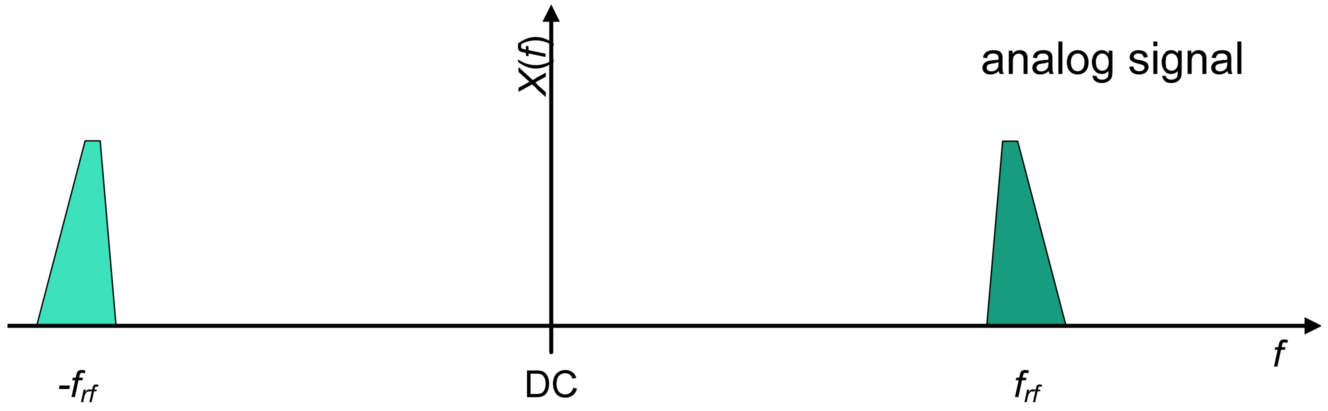
don’t forget
negative
frequencies

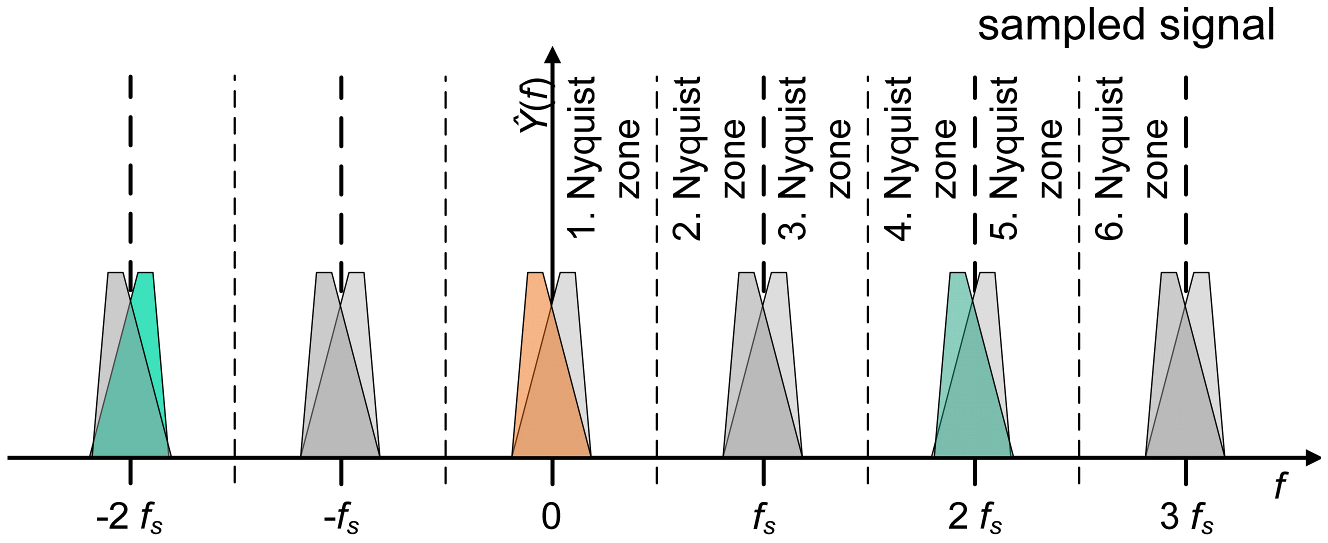




2. Analog-to-Digital Conversion

Ideal Sampling





simple

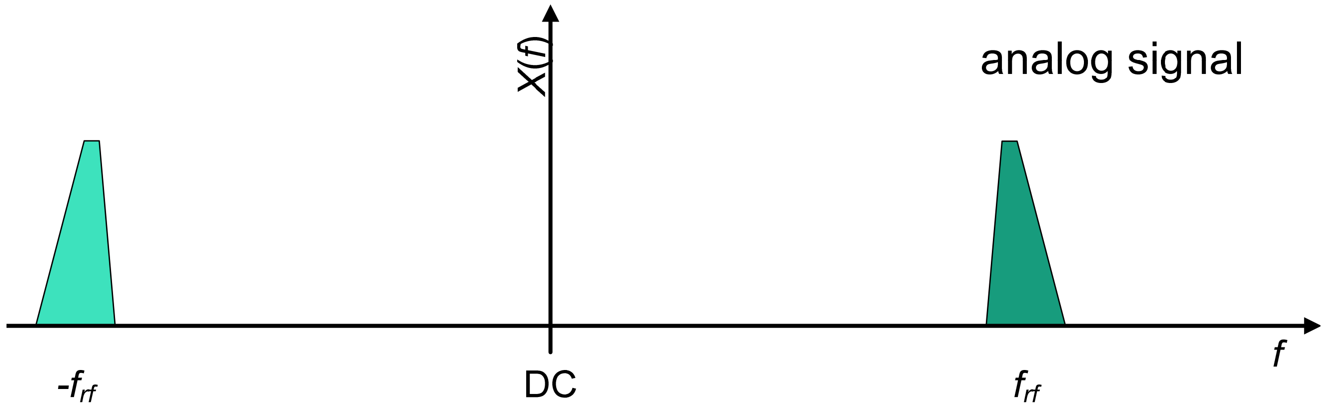
frequency shift

⇩

aliasing

2. Analog-to-Digital Conversion

Ideal Sampling

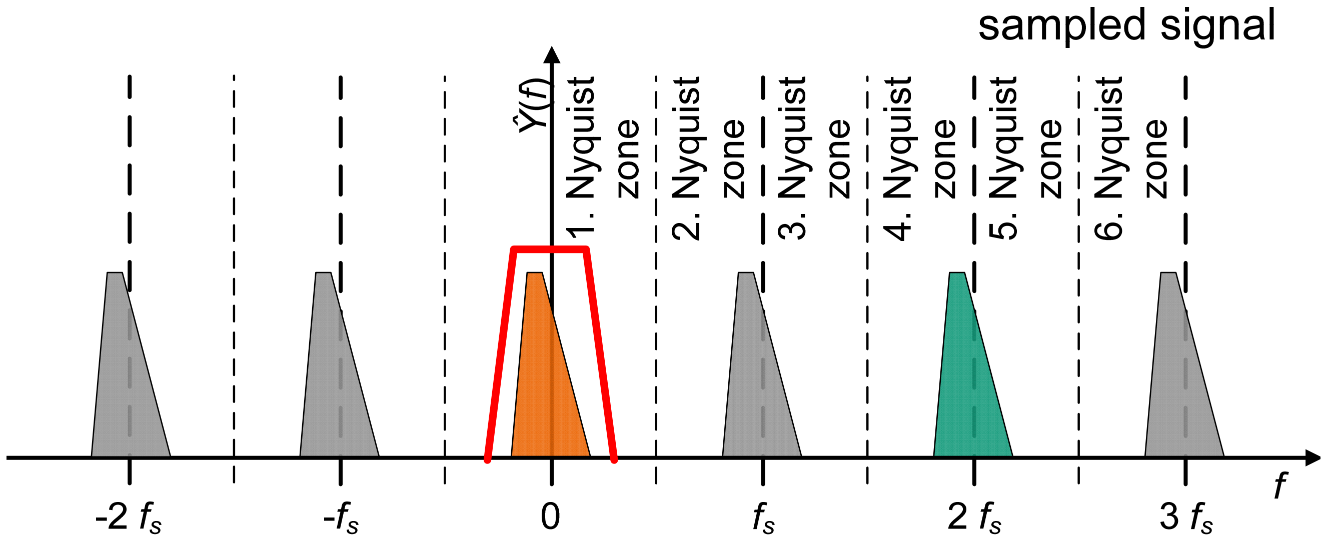


complex

frequency shift

+

low pass filter



2. Analog-to-Digital Conversion

Ideal Quantization

Power of quantization error:

$$P_q = \sigma^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e_k^2(x)dx = \frac{\Delta^2}{12},$$

with e_k is the uniformly distributed, zero mean quantization error

Uniformly distributed input signal:

$$\mathrm{SQNR} = 10\log_{10}\left(\frac{P_s}{P_q}\right)\mathrm{dB} = 10\log_{10}\left(\frac{{V_{FS}}^2}{\Delta^2}\right)\mathrm{dB} = 6{,}02N\ \mathrm{dB}$$

Arbitrary input signal:

$$\mathrm{SQNR} = 6{,}02\mathrm{N} + 4.77 - 10\log_{10}(\eta)\mathrm{dB}$$

with η is the peak-to-average power ratio

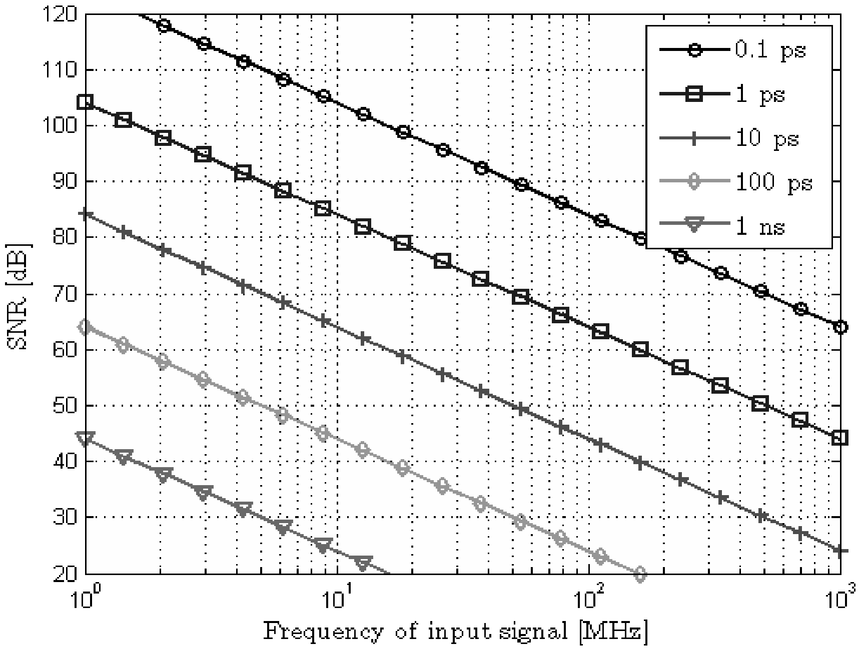
Full scale sinusoidal signal:

$$\mathrm{SQNR} = 6{,}02N + 1{,}76\ \mathrm{dB}$$

2. Analog-to-Digital Conversion
Noise Sources

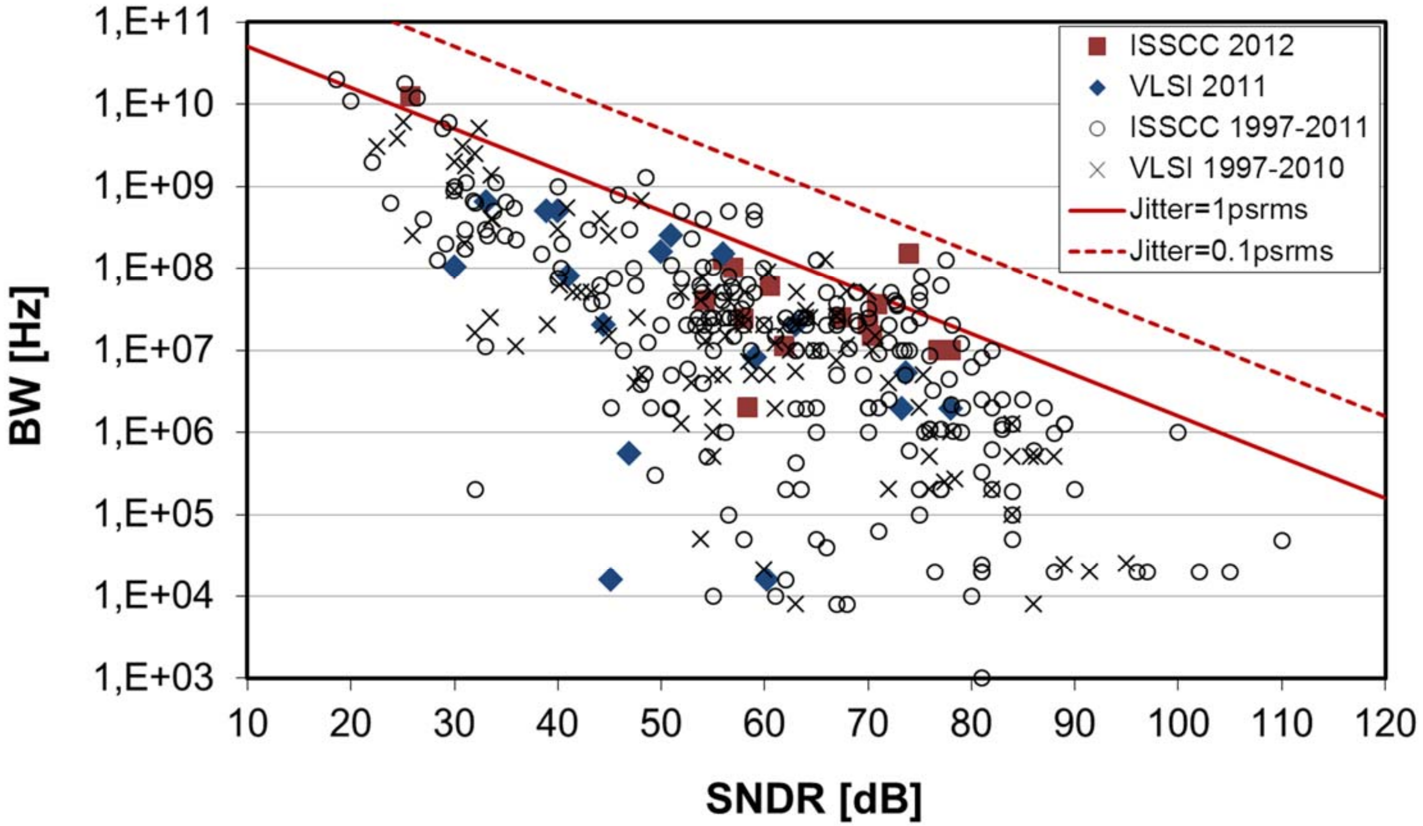
Four main noises sources:

1. **Quantization noise**
2. **Thermal noise**
   generated at the analog frontend of the ADC by temperature dependent random movement of electrons in resistive components
3. **Jitter**
   due to imperfections of the sample and hold circuitry (**aperture jitter**) and phase noise of the external sample clock (**clock jitter**)
4. **Comparator ambiguity**
   based on the finite regeneration time constant of the comparators



SNR degradation due to jitter

2. Analog-to-Digital Converter
State-of-the-Art in Research



Source: B. Murmann, "ADC Performance Survey 1997-2012," [Online]. available: http://www.stanford.edu/~murmann/adcsurvey.html.

2. Analog-to-Digital Converter
State-of-the-Art in Commercial Available Components

Type	Resolution	Sample Rate [MS/s]	Bandwidth [MHz]	SNR [dBFS]	SFDR [dBc]	SINAD [dBFS]	ENOB	Power consumption [mW]
ADC12D1800	12	**3600**	2700	58.6	68.1	57.7	9.3	2260
KAD5512P	12	500	1300	65.9	87.3	65.7	10.6	432
ADS5474	14	400	1440	70.2	86	68.9	11.2	2500
KAD5514	14	250	950	69.4	89.9	69.1	11.2	390
AD9467	16	250	730	76	93	76	12.3	1330
ADS4149	14	200	800	72.9	80	72.1	11.7	265
ADC16V130	16	160	1400	78	94			1300
LTC2209	16	160	700	77.1	**100**	77		1450
ADC4146	16	160	800	72	87	71.8	11.5	**200**
AD9261-10	16	160	**10**	**82.5**	87		13.5	375
AD9265	16	125	650	79	93	78.7	12.8	391
AD9650	16	105	500	**82**	90	82	13.2	328

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3. Dynamic Range Enhancement Techniques

Overview

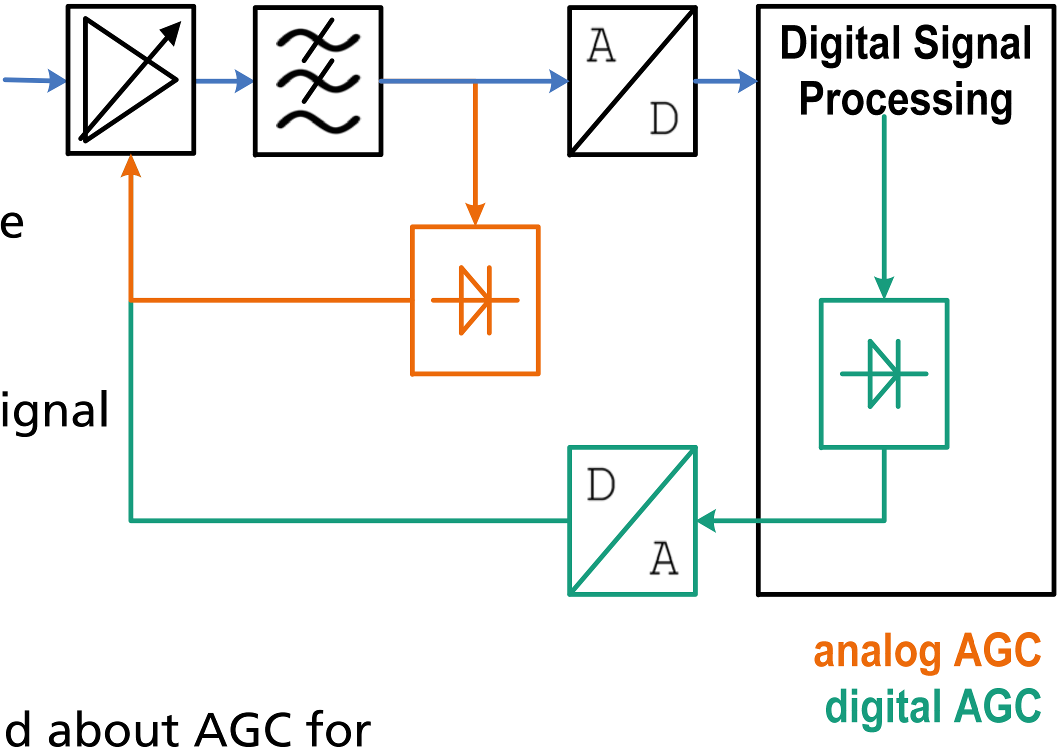
There are a lot of measures known improving SNR and SFDR of the ADC on chip level. These measures are not subject of this talk.

➡ **Limitation to board level technologies**
(not the ADC component itself)

- automatic gain control (AGC)
- non-uniform quantization
- time-interleaved ADC
- signal averaging

3. Dynamic Range Enhancement Techniques

Automatic Gain Control (AGC)

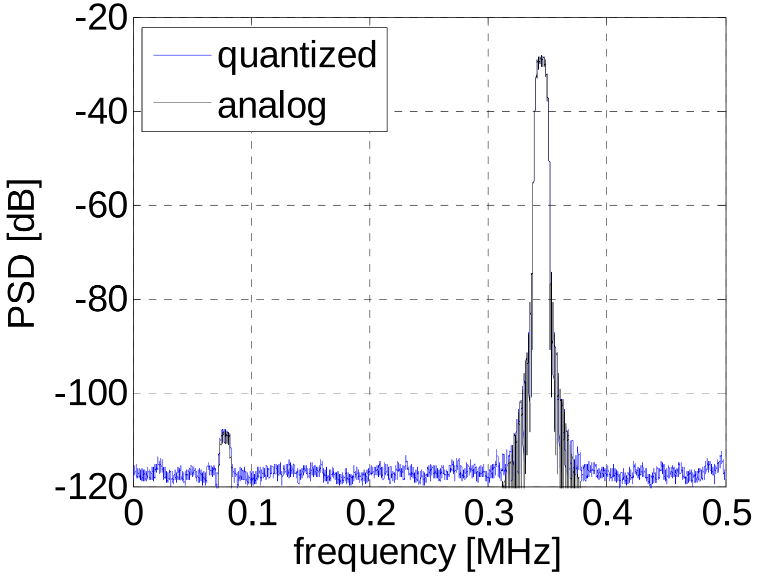


- gain might be defined by interferers
- Strong interferer can push wanted signal into the noise floor of the ADC
- every change of the gain causes interference to the signal and should be avoided
- control strategy important, e.g. for a dynamic interference scenario
- only little information found about AGC for broadband RX in literature

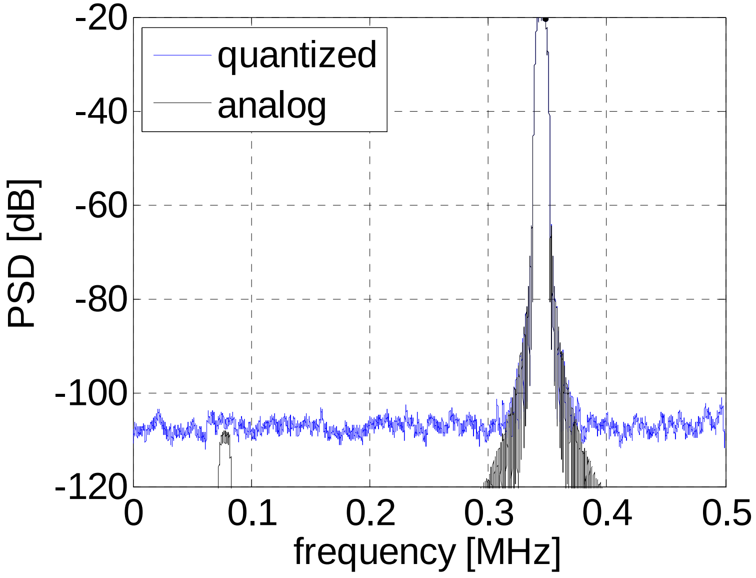
3. Dynamic Range Enhancement Techniques
Automatic Gain Control (AGC) – Simulation Results

Impact of a strong interferer:

- 10 dB higher interferer (right) causing 10 dB gain reduction by AGC
- wanted signal is hidden by quantization noise of the 12-bit ADC



weak signal within ADC dynamic range

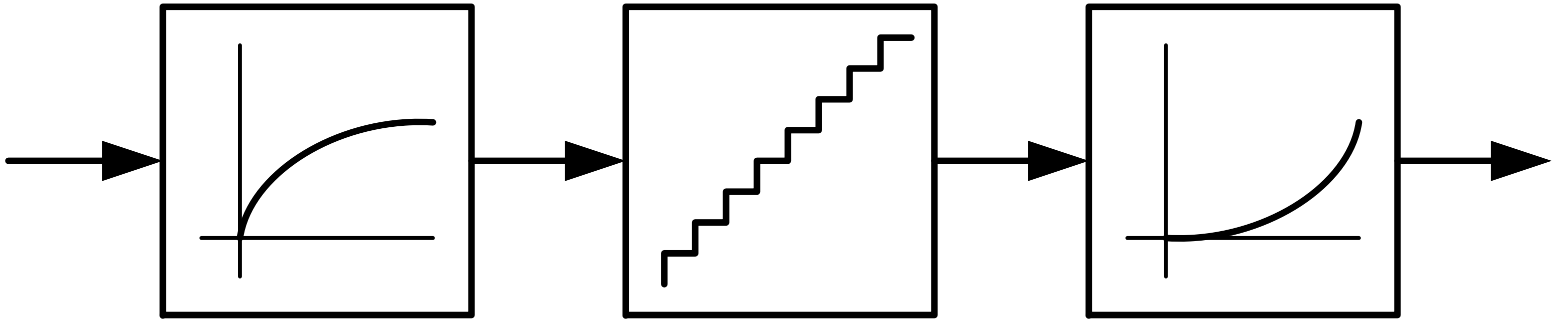


ADC dynamic range not sufficient

3. Dynamic Range Enhancement Techniques

Non-uniform Quantization - Principle

- non-uniform quantization for compression of strong signals and at the same time fine resolution of weak signals
- used e.g. for audio signal quantization
- e.g. µ-law compression: $y(x) = \operatorname{sgn}(x)\dfrac{\log(1+\mu|x|)}{\log(1+\mu)}$



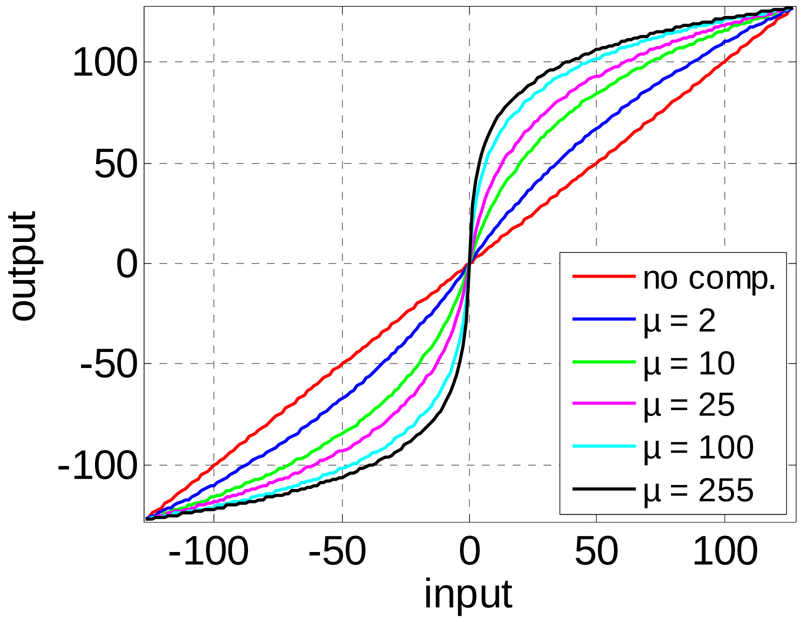
compression

uniform quantization

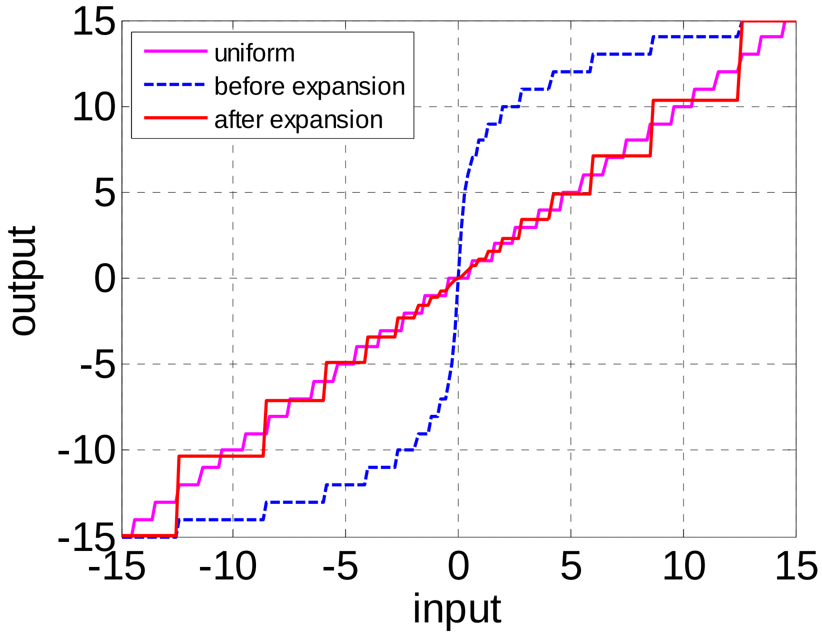
expansion

3. Dynamic Range Enhancement Techniques

Non-uniform Quantization - µ-law Approach



compression characteristic of an 8-bit µ-law quantizer (µ = 0 … 255)

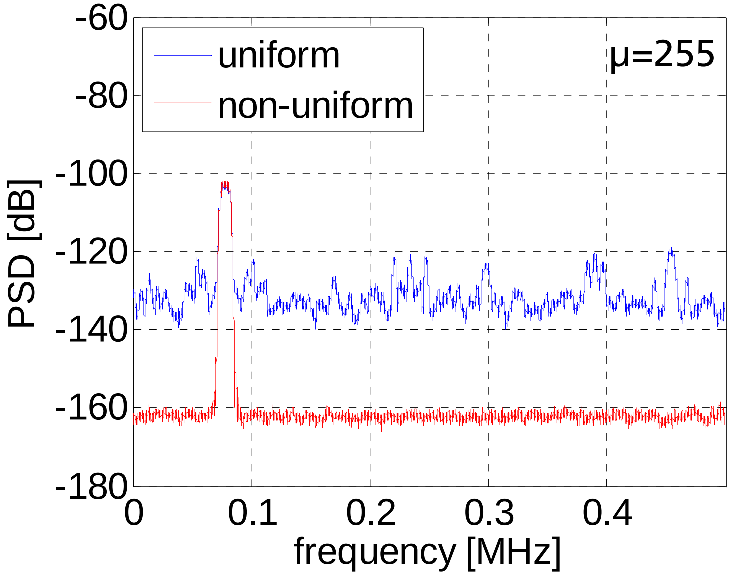


transfer and error characteristic of a 5-bit µ-law quantizer (µ = 255)

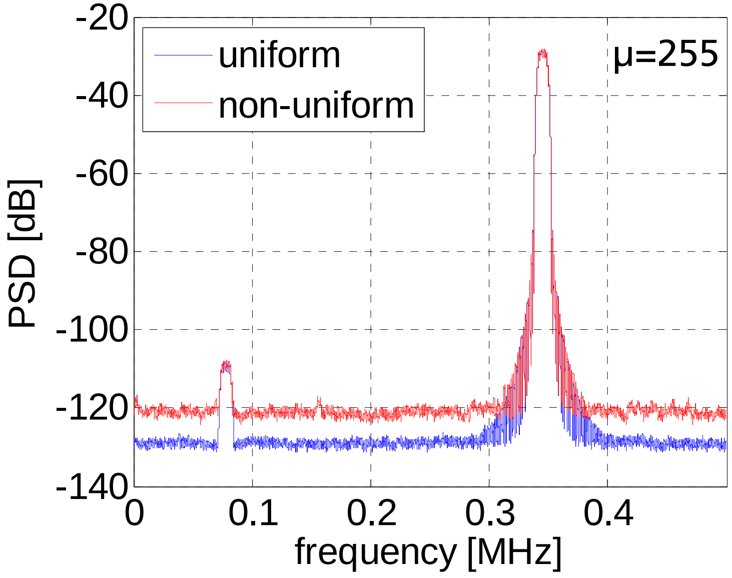
3. Dynamic Range Enhancement Techniques
Non-uniform Quantization – Simulation Results

Benefit in Software Defined Radio receivers is questionable:

- if weak signal is superimposed on the strong interferer => only poor resolution of the weak signal => SNR reduces



quantization of weak signal



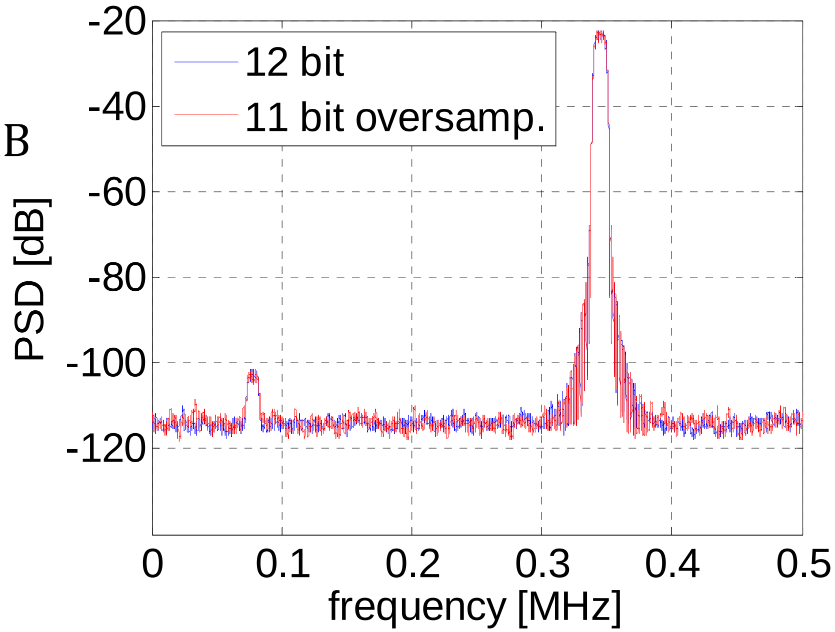
quantization of weak and strong signal

3. Dynamic Range Enhancement Techniques
Oversampling

If the noise power is white within one Nyquist zone, the SNR improves with respect to the channel bandwidth (BW) according to

$$\mathrm{SNR}_{\mathrm{channel}} = \mathrm{SNR} + 10\log_{10}\left(\frac{f_S}{2 \cdot BW}\right)\ \mathrm{dB}$$

Oversampling with factor 4
improves the SNR by 6 dB ≙ 1 bit



SNR improvement with oversampling

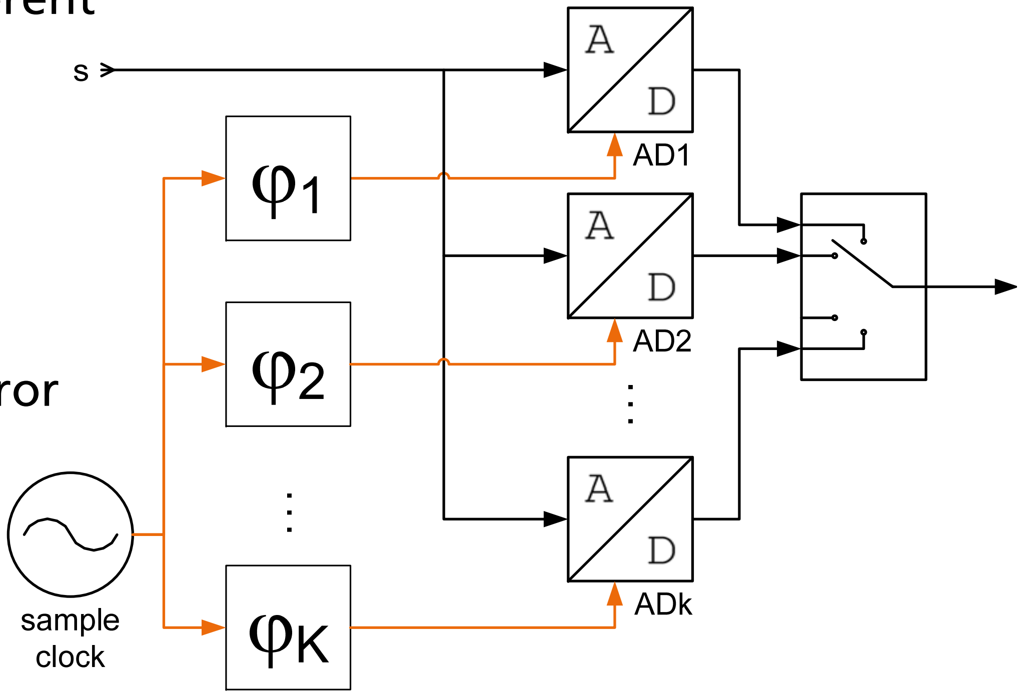
3. Dynamic Range Enhancement Techniques
Time-interleaved ADCs

To increase the sample-rate of the ADC:

- 2…k parallel ADCs, clocked with the same frequency but different phase

$$\varphi_k = 2\pi \cdot \left(\frac{k-1}{K}\right)$$

- With 0.02% gain or phase error the max. SFDR is 74 dB
- Post-processing for error correction



3. Dynamic Range Enhancement Techniques
Signal Averaging with Parallel ADCs

Idea:

- signal sums coherently, noise is uncorrelated and sums on an RMS basis => gain of 3 dB in SNR
- Seifert & Narda: $$\mathrm{ENOB} = N - \frac{1}{2}\log_2\left(\frac{P_N}{P_q}\right) = N - \frac{1}{2}\log_2\left(\frac{P_q + P_d + P_{ADC}}{P_q}\right)$$

  N = nominal Bits, P_N = complete noise power, P_q = quantization noise, P_d = power of small scale dither, P_{ADC} = residual noise (thermal, jitter)
- With $P_d = P_q$ => for 1 ADC: $$\mathrm{ENOB} = N - \frac{1}{2}\log_2\left(\frac{2P_q + P_{ADC}}{P_q}\right)$$
- For k parallel ADCs: $$\mathrm{ENOB} = N - \frac{1}{2}\log_2\left(\frac{2k^2P_q + kP_{ADC}}{k^2P_q}\right) = N - \frac{1}{2}\log_2\left(2 + \frac{P_{ADC}}{kP_q}\right)$$

3. Dynamic Range Enhancement Techniques

Signal Averaging with Parallel ADCs

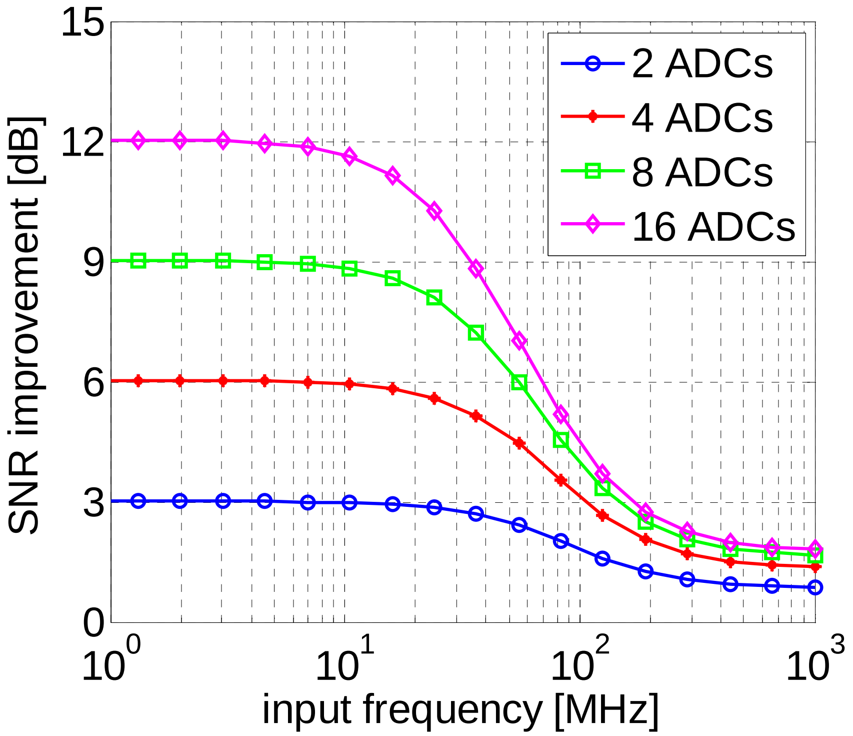
- According to Lauritzen:

$$\mathrm{SNR} = \left(\frac{1}{k \cdot \mathrm{SNR}_{therm}} + \frac{(\omega \cdot \sigma_m)^2}{k} + (\omega \cdot \sigma_\mu)^2 \right)^{-1}$$

σ_m = aperture jitter and
σ_μ = clock jitter

- Clock jitter is correlated and limits the improvement with higher input frequency

- Example:
aperture jitter = 75 fs
clock jitter = 100 fs
SNR of the single ADC = 82 dB



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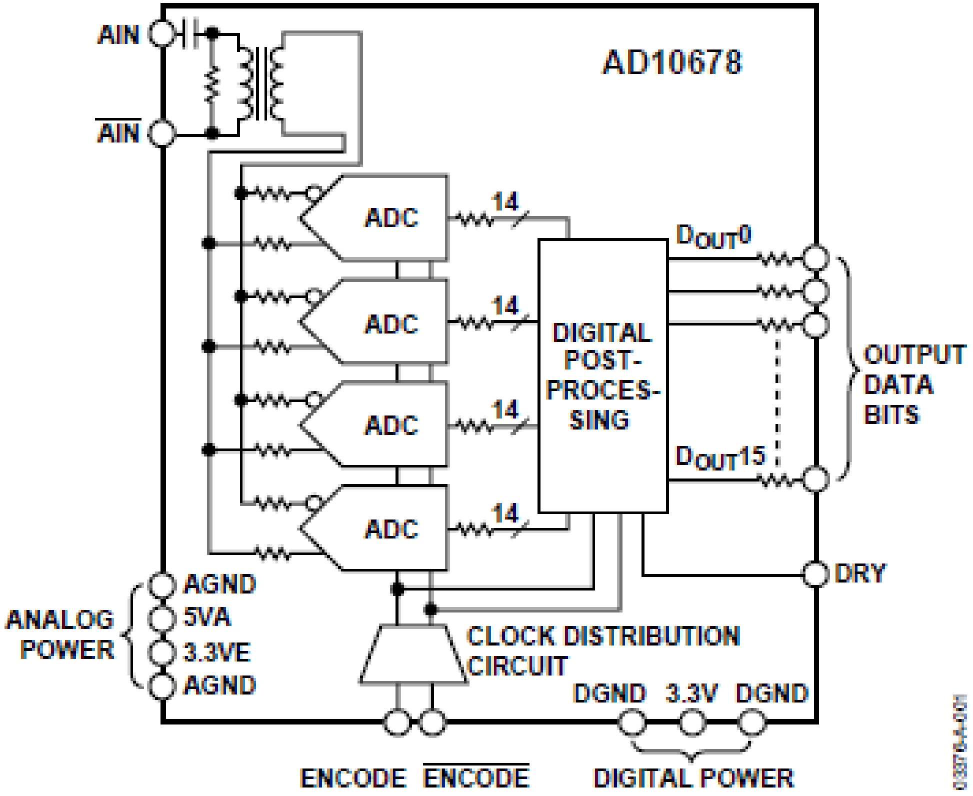
3. Dynamic Range Enhancement Techniques
Signal Averaging with Parallel ADCs

- 4 parallel ADCs AD6645 implemented in the AD10678

- AD6645, 80 MSPS
  SNR @ 15.5 MHz: 75 dB
  SNR @ 30.5 MHz: 74.5 dB
  SFDR @ 30.5 MHz: 93 dB

- AD10678
  SNR @ 10 MHz: 80.5 dB
  SNR @ 30 MHz: 80.2 dB
  SFDR @ 30 MHz: 94.2 dB



3. Conclusions

- Extreme dynamic range requirements for Software Radios caused by collocated transmitters
- Analog-to-digital converter technology improves but is not able to handle these requirements
- AGC will be necessary also in future, but cannot provide the necessary dynamic range in the presence of a strong interferer
- Signal averaging with parallel ADCs can improve the dynamic range of the analog-to-digital conversion, but is limited by jitter to frequencies below 100 MHz